

# Model Checking I

alias

## Reactive Systems Verification

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### Topics

- Parallelism and Communication
- Synchronous Message Passing
- Examples

### Material

Reading:

Chapter 2 of the book, pages 47–53.

More:

The slides in the following pages are taken from the material of the course “Introduction to Model Checking” held by Prof. Dr. Ir. Joost-Pieter Katoen at Aachen University.

# Operators for parallelism and communication

PC2.2-16

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  - \* operator  $\parallel_{Syn}$  for TS
  - \* interleaving for independent actions
  - \* synchronization over actions in *Syn*

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- channel systems

communication via shared variables + via channels
- synchronous product

# Synchronous message passing

PC2.2-17

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PC2.2-17

$\mathcal{T}_1 = (S_1, Act_1, \rightarrow_1, \dots)$ ,  $\mathcal{T}_2 = (S_2, Act_2, \rightarrow_2, \dots)$  TS

$Syn \subseteq Act_1 \cap Act_2$  set of synchronization actions

# Synchronous message passing

PC2.2-17

$$\mathcal{T}_1 = (S_1, Act_1, \rightarrow_1, \dots), \mathcal{T}_2 = (S_2, Act_2, \rightarrow_2, \dots) \text{ TS}$$

*Syn*  $\subseteq Act_1 \cap Act_2$  set of synchronization actions

composite transition system:

$$\mathcal{T}_1 \parallel_{Syn} \mathcal{T}_2 = (S_1 \times S_2, Act_1 \cup Act_2, \rightarrow, \dots)$$

for modeling the concurrent execution of  $\mathcal{T}_1$  and  $\mathcal{T}_2$   
with **synchronization** over all actions in *Syn*

# Synchronous message passing

PC2.2-17

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$$\frac{s_1 \xrightarrow{\alpha} s'_1}{\langle s_1, s_2 \rangle \xrightarrow{\alpha} \langle s'_1, s_2 \rangle} \qquad \frac{s_2 \xrightarrow{\alpha} s'_2}{\langle s_1, s_2 \rangle \xrightarrow{\alpha} \langle s_1, s'_2 \rangle}$$

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# Mutual exclusion

PC2.2-18

by synchronous message passing

# Mutual exclusion

PC2.2-18

by synchronous message passing using an arbiter

# Mutual exclusion with an arbiter

PC2.2-18

protocol for process  $P_i$

```
LOOP FOREVER DO
    noncritical actions
    request
    critical section
    release
    noncritical actions
OD
```

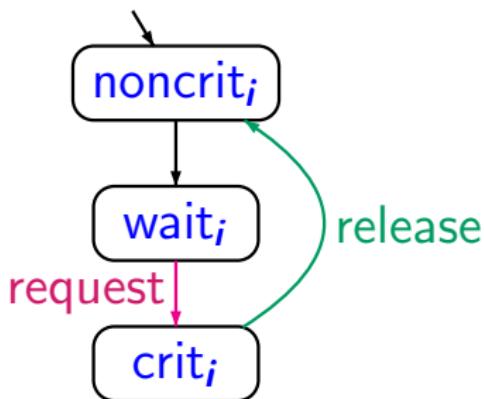
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PC2.2-18

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transition system  $\mathcal{T}_i$



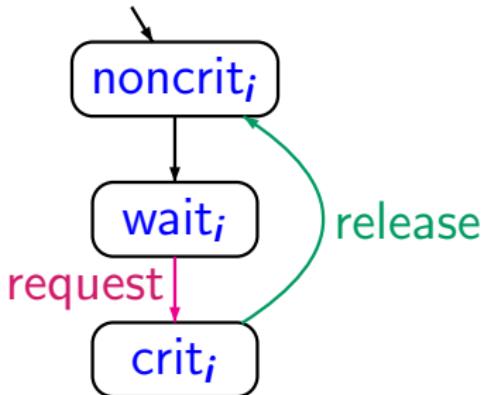
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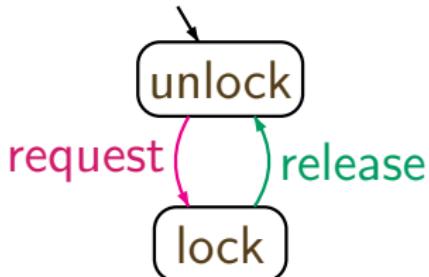
transition system  $\mathcal{T}_i$



**Arbiter:**

selects nondeterministically  
a synchronization partner

$T_1$  or  $T_2$



# Mutual exclusion with an arbiter

PC2.2-19

$(\mathcal{T}_1 \ ||| \mathcal{T}_2) \ \|_{Syn} \text{ } Arbiter$  where  $Syn = \{\text{request}, \text{release}\}$

# Mutual exclusion with an arbiter

PC2.2-19

$(\mathcal{T}_1 \parallel\!\!\!|| \mathcal{T}_2) \parallel_{Syn} \text{Arbiter}$  where  $Syn = \{\text{request}, \text{release}\}$



“pure”  
interleaving  
for TS

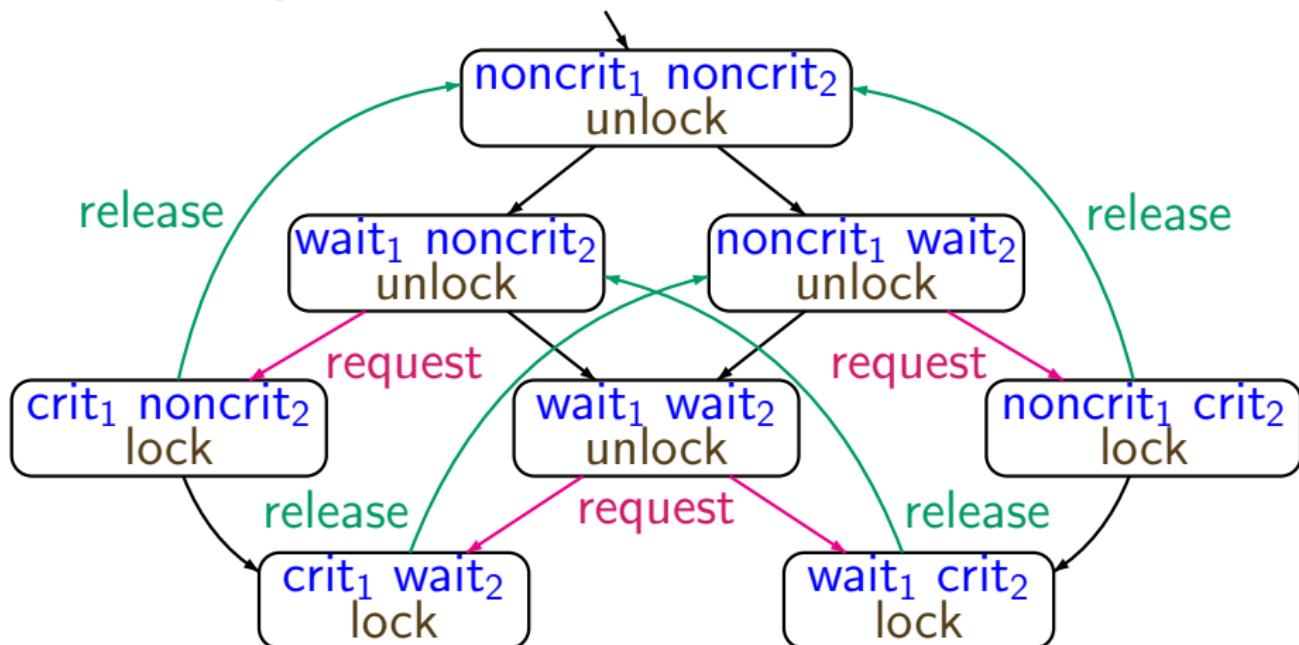


handshaking  
for actions  
**request** and **release**

# Mutual exclusion with an arbiter

PC2.2-19

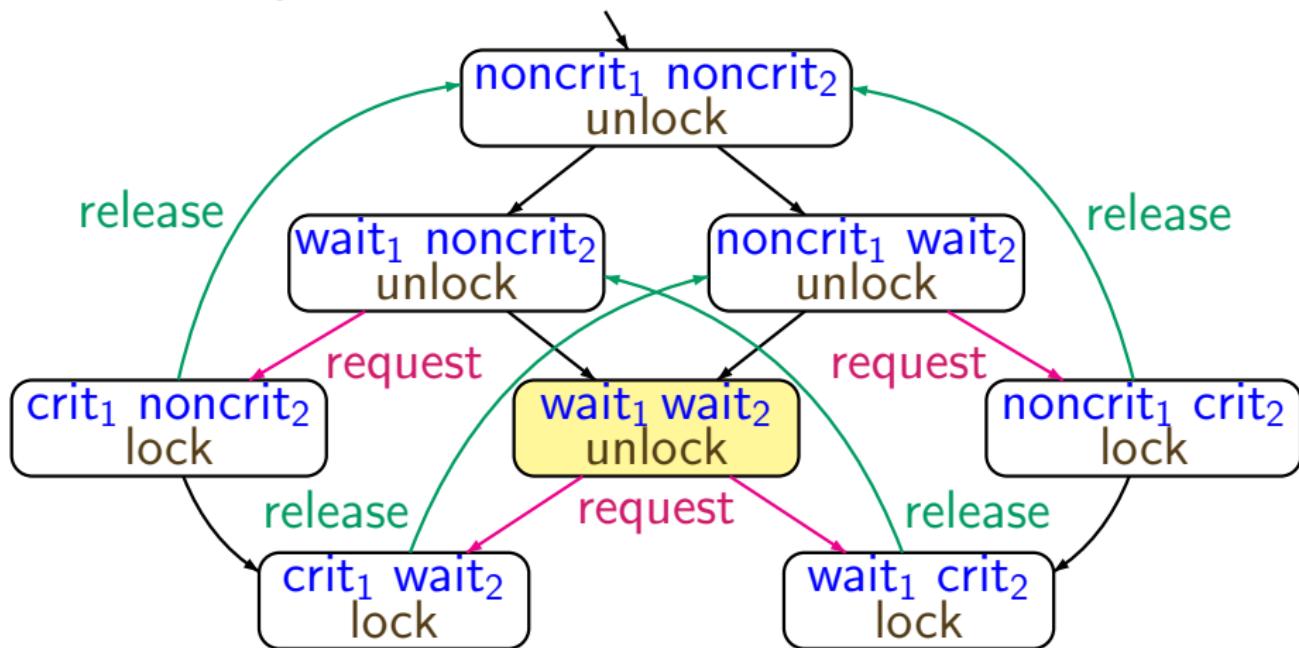
$(T_1 \parallel\!\!\| T_2) \parallel_{Syn} \text{Arbiter}$  where  $Syn = \{\text{request}, \text{release}\}$



# Mutual exclusion with an arbiter

PC2.2-19

$(T_1 \parallel\!\!\| T_2) \parallel_{Syn} \text{Arbiter}$  where  $Syn = \{\text{request}, \text{release}\}$



*nondeterministic choice:* who enters the critical section?

# Synchronous message passing

PC2.2-HANDSHAKING-GENERALIZATION

synchronization operator  $\parallel_{Syn}$  for  
three or more processes

# Synchronous message passing

PC2.2-HANDSHAKING-GENERALIZATION

$$\begin{array}{lcl} T_1 & = & (S_1, \textcolor{violet}{Act}_1, \rightarrow_1, \dots) \\ T_2 & = & (S_2, \textcolor{brown}{Act}_2, \rightarrow_2, \dots) \\ T_3 & = & (S_3, \textcolor{blue}{Act}_3, \rightarrow_3, \dots) \\ T_4 & = & (S_4, \textcolor{red}{Act}_4, \rightarrow_4, \dots) \\ \vdots & & \vdots \end{array} \quad \left. \right\} \text{transition systems}$$

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for  $Syn \subseteq Act_1 \cup Act_2 \cup Act_3 \cup Act_4 \cup \dots$

$$\begin{aligned} \mathcal{T}_1 \parallel_{Syn} \mathcal{T}_2 \parallel_{Syn} \mathcal{T}_3 \parallel_{Syn} \mathcal{T}_4 \parallel_{Syn} \dots &\stackrel{\text{def}}{=} \\ \left( ((\mathcal{T}_1 \parallel_{Syn} \mathcal{T}_2) \parallel_{Syn} \mathcal{T}_3) \parallel_{Syn} \mathcal{T}_4 \right) \parallel_{Syn} \dots \end{aligned}$$

# Synchronous message passing

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or any other order of parenthesis

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where, e.g.,  $\mathcal{T}_1 \parallel_{Syn} \mathcal{T}_2 \stackrel{\text{def}}{=} \mathcal{T}_1 \parallel_H \mathcal{T}_2$

with  $H = Syn \cap \textcolor{violet}{Act}_1 \cap \textcolor{blue}{Act}_2$

# Parallel operator $\parallel$

PC2.2-OP-PAR

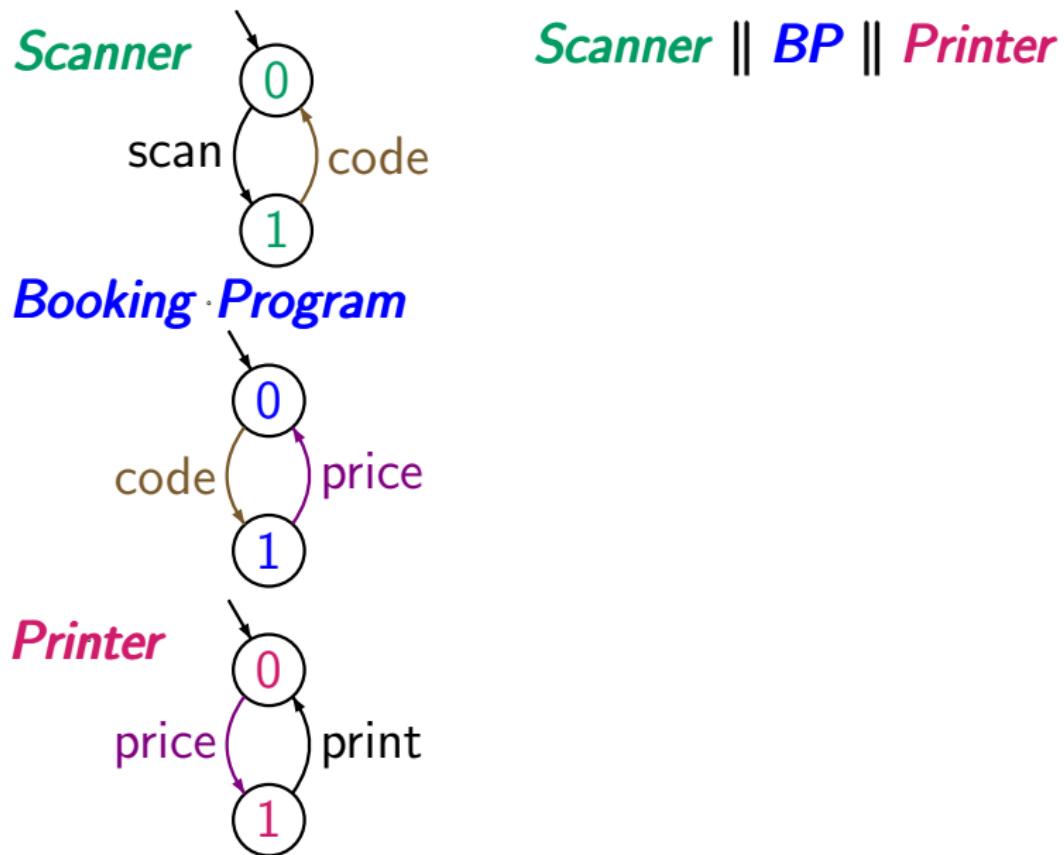
$$\begin{array}{ll} \mathcal{T}_1 = (\mathcal{S}_1, \mathcal{A}\mathcal{C}_1, \rightarrow_1, \dots) & \text{transition systems s.t.} \\ \mathcal{T}_2 = (\mathcal{S}_2, \mathcal{A}\mathcal{C}_2, \rightarrow_2, \dots) & \mathcal{A}\mathcal{C}_i \cap \mathcal{A}\mathcal{C}_j \cap \mathcal{A}\mathcal{C}_k = \emptyset \\ \mathcal{T}_3 = (\mathcal{S}_3, \mathcal{A}\mathcal{C}_3, \rightarrow_3, \dots) & \text{if } i, j, k \text{ are pairwise} \\ \mathcal{T}_4 = (\mathcal{S}_4, \mathcal{A}\mathcal{C}_4, \rightarrow_4, \dots) & \text{distinct} \\ \vdots & \vdots \end{array}$$

$$\begin{aligned} \mathcal{T}_1 \parallel \mathcal{T}_2 \parallel \mathcal{T}_3 \parallel \mathcal{T}_4 \parallel \dots &\stackrel{\text{def}}{=} \\ (((\mathcal{T}_1 \parallel_{Syn_{1,2}} \mathcal{T}_2) \parallel_{Syn_{1,2,3}} \mathcal{T}_3) \parallel_{Syn_{1,2,3,4}} \mathcal{T}_4) \dots \end{aligned}$$

$$\begin{array}{lll} \text{where } Syn_{1,2} & = & \mathcal{A}\mathcal{C}_1 \cap \mathcal{A}\mathcal{C}_2 \\ Syn_{1,2,3} & = & (\mathcal{A}\mathcal{C}_1 \cup \mathcal{A}\mathcal{C}_2) \cap \mathcal{A}\mathcal{C}_3 \\ Syn_{1,2,3,4} & = & (\mathcal{A}\mathcal{C}_1 \cup \mathcal{A}\mathcal{C}_2 \cup \mathcal{A}\mathcal{C}_3) \cap \mathcal{A}\mathcal{C}_4 \\ \vdots & & \vdots \end{array}$$

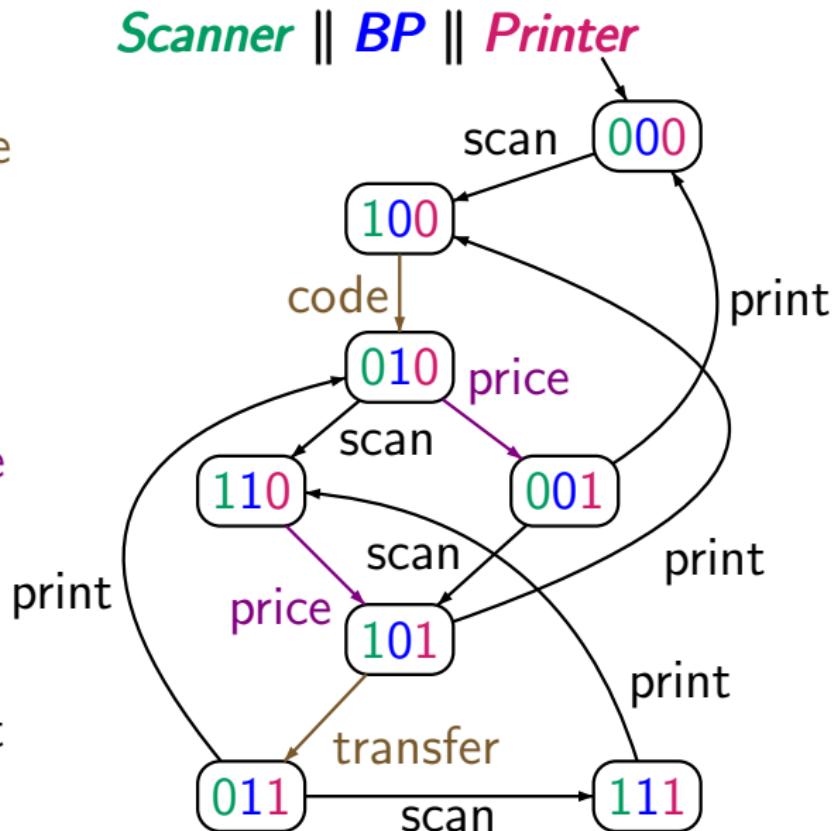
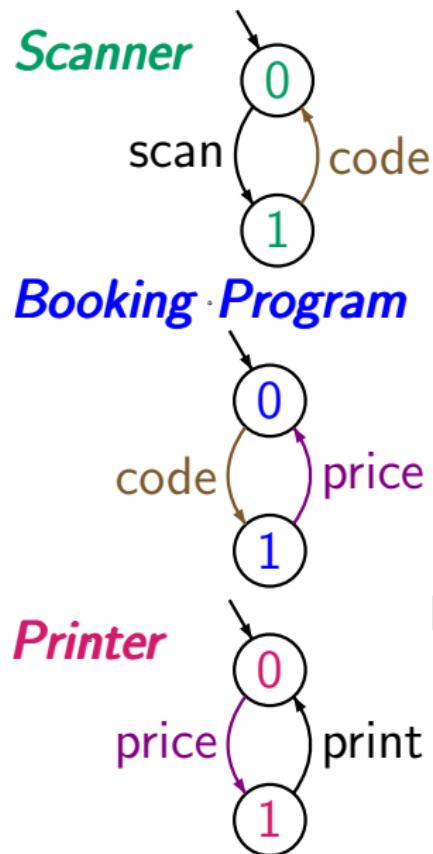
# Booking system in supermarket

PC2.2-21A



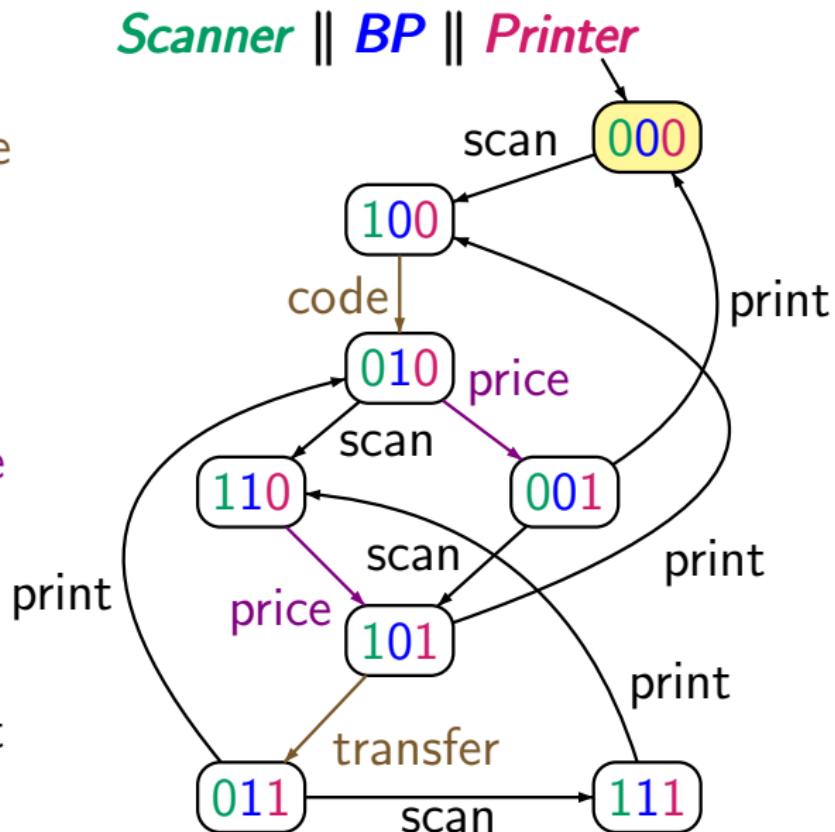
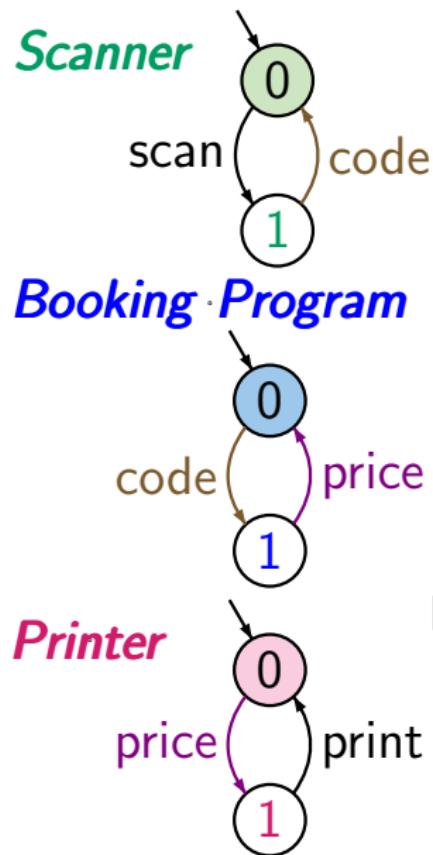
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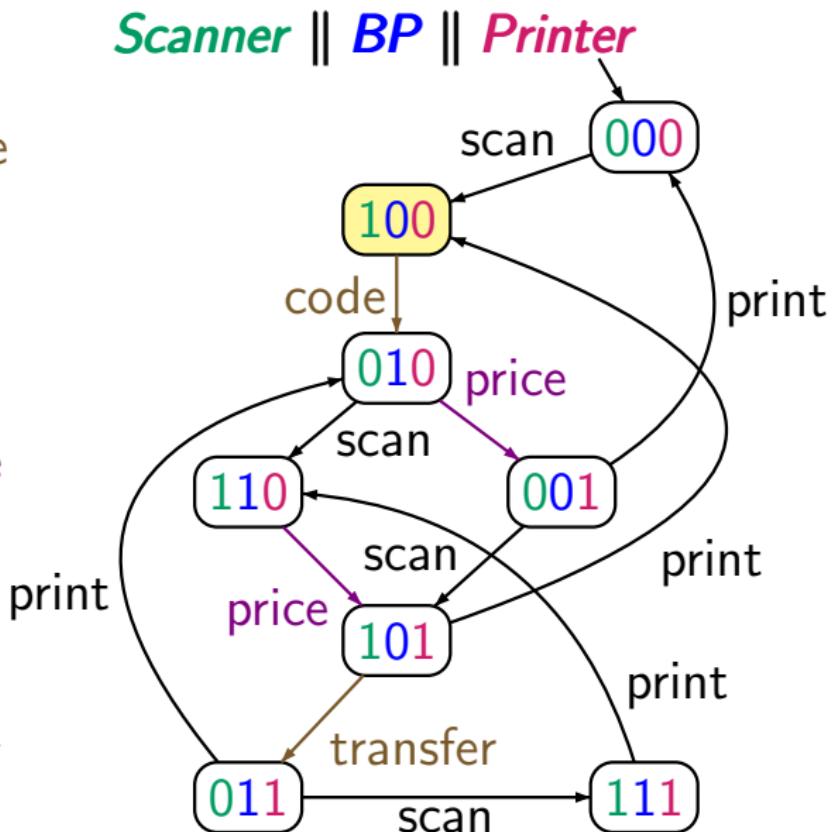
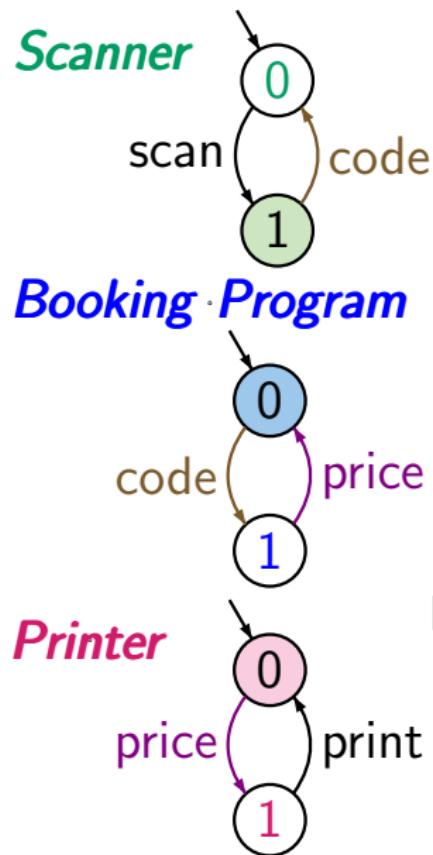
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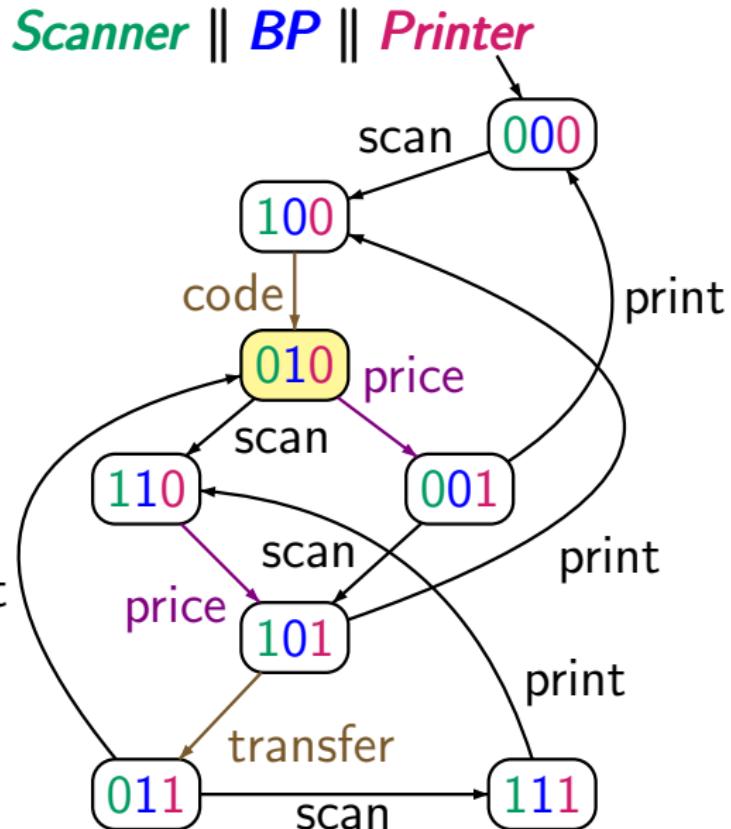
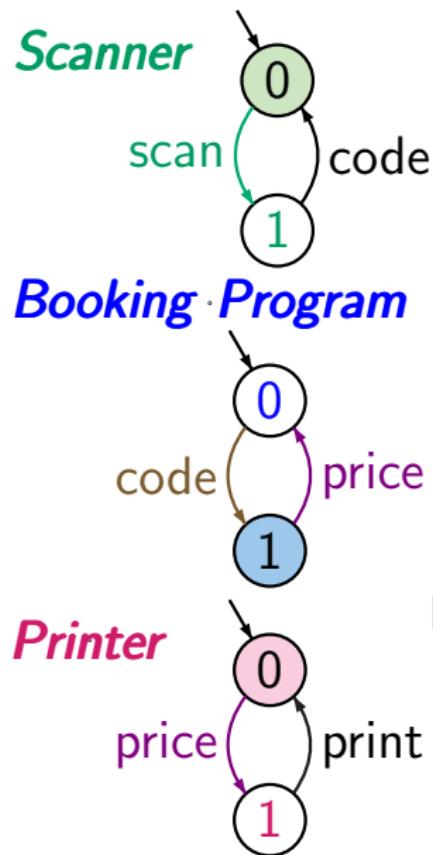
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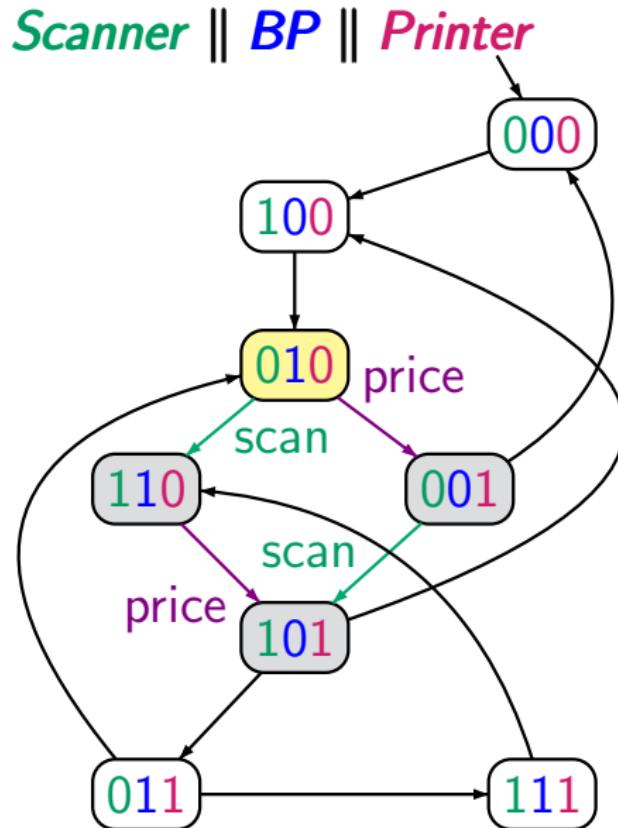
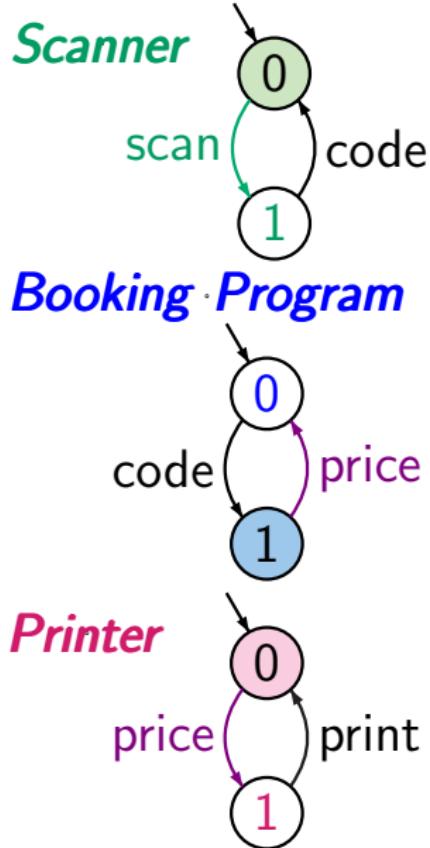
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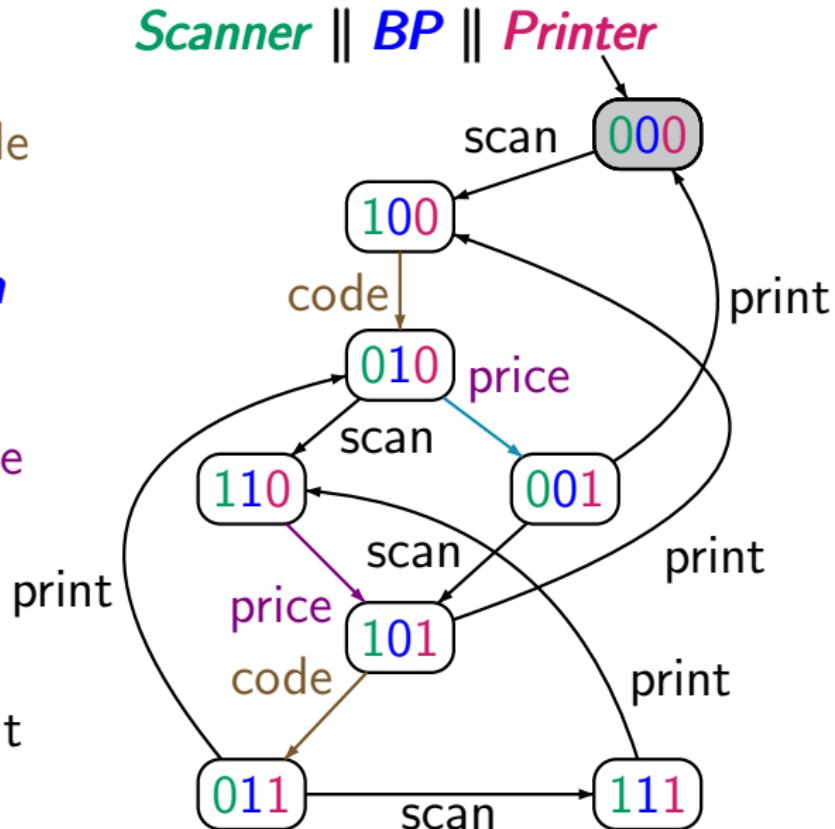
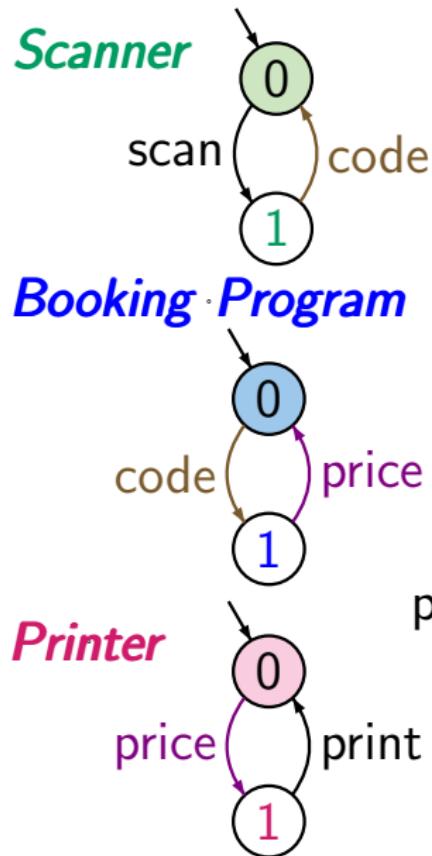
# Interleaving

PC2.2-21A



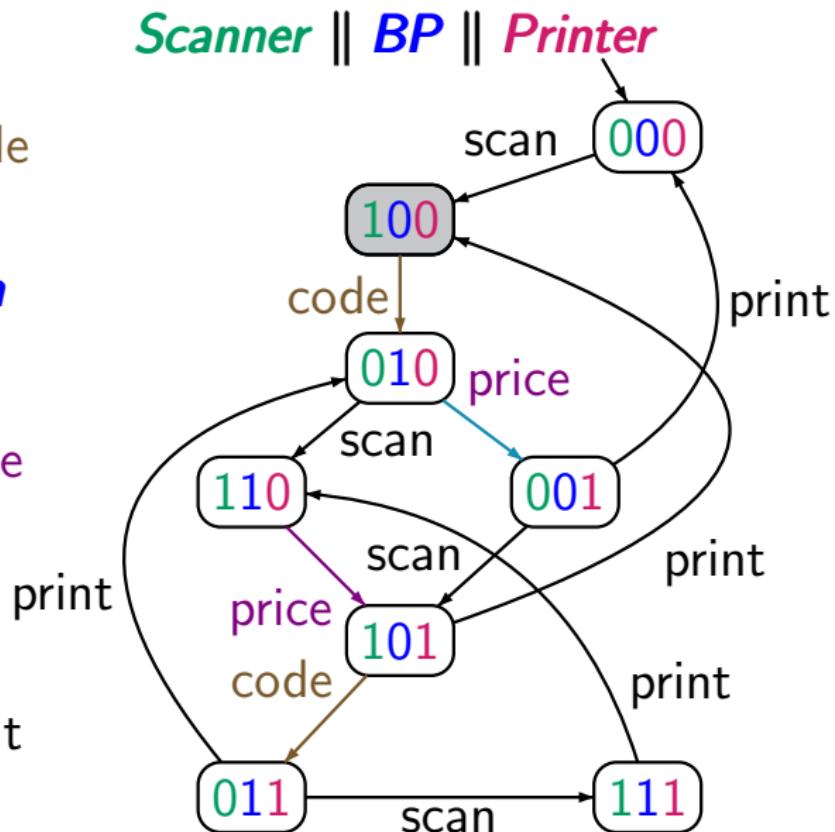
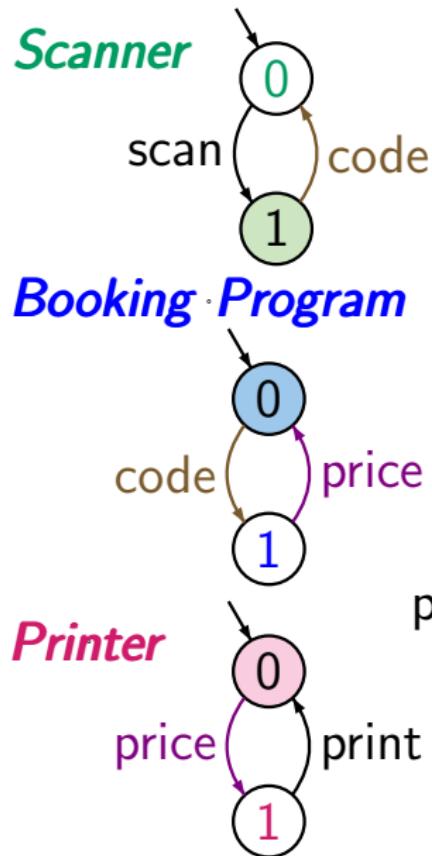
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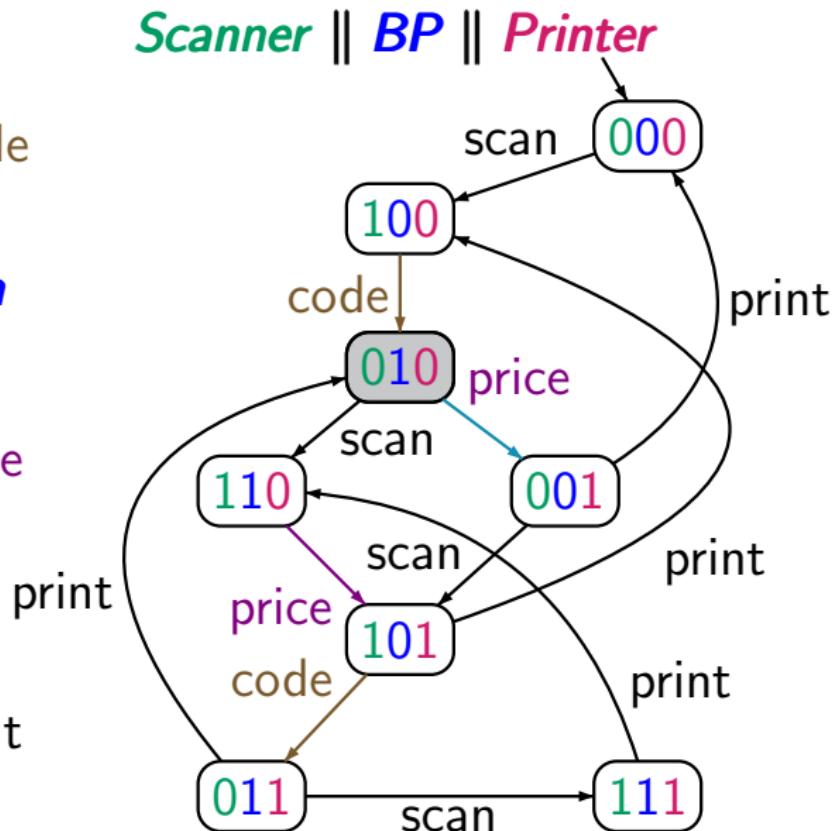
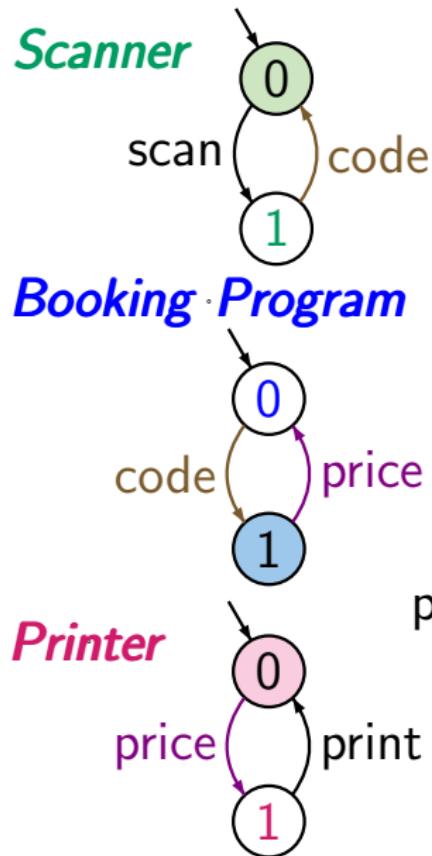
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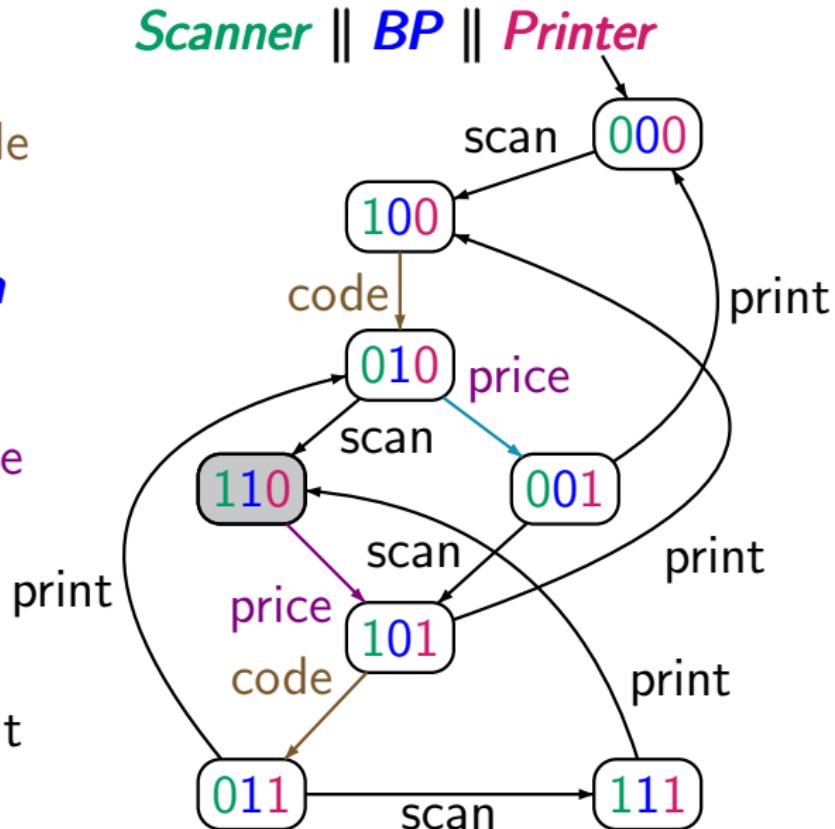
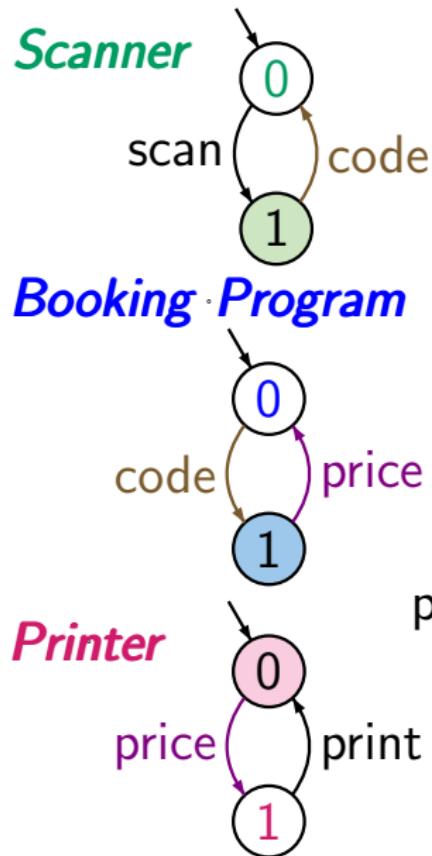
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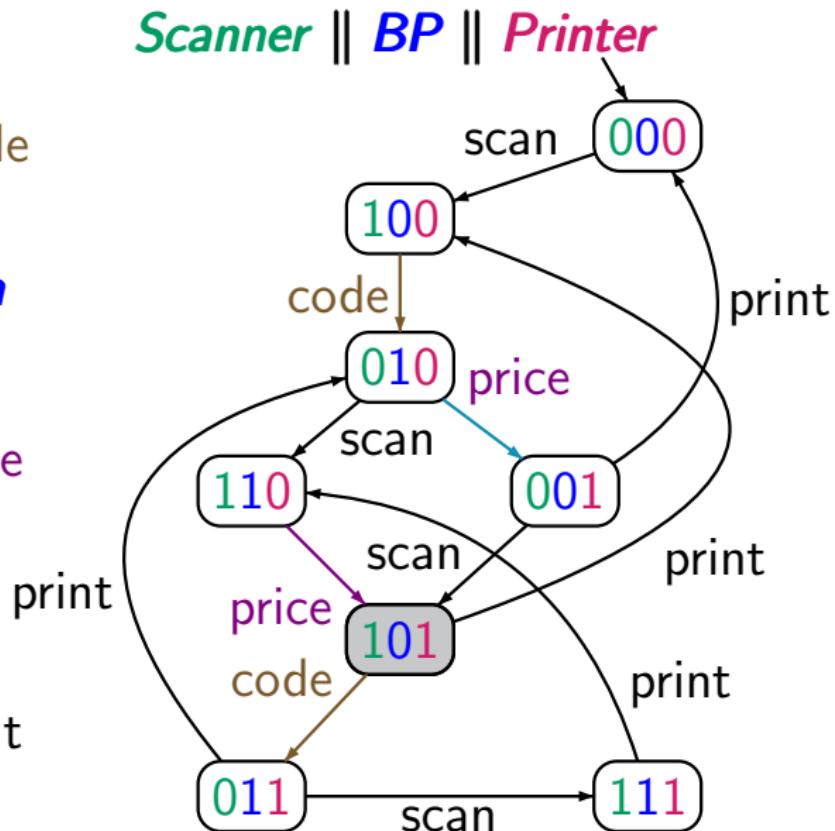
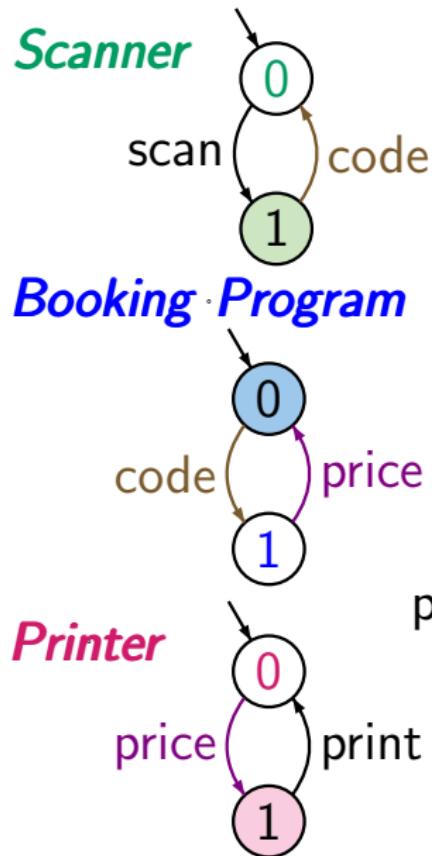
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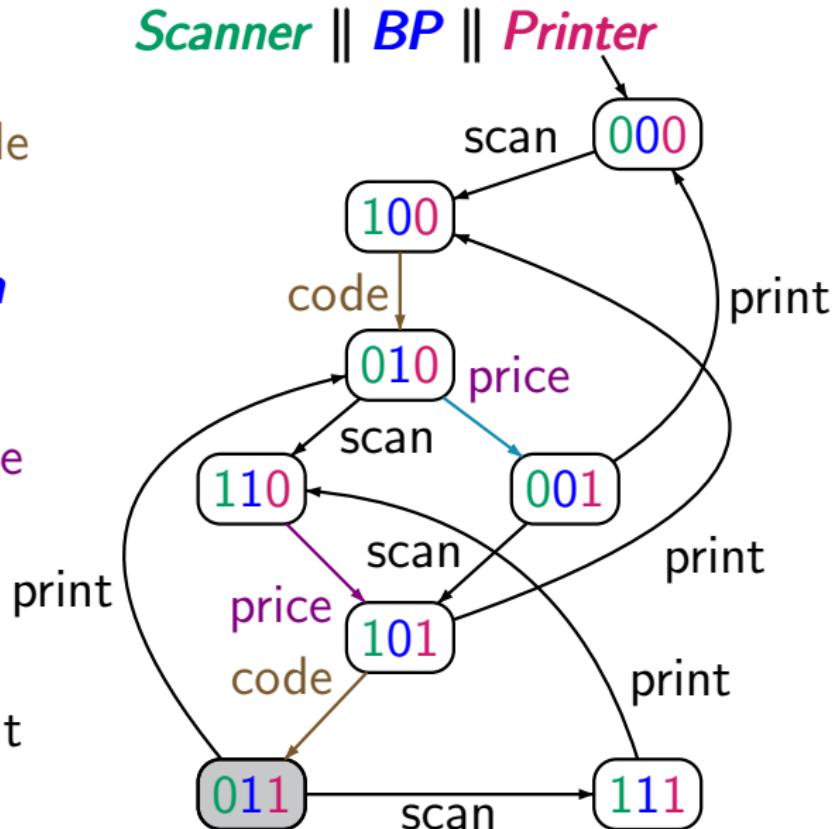
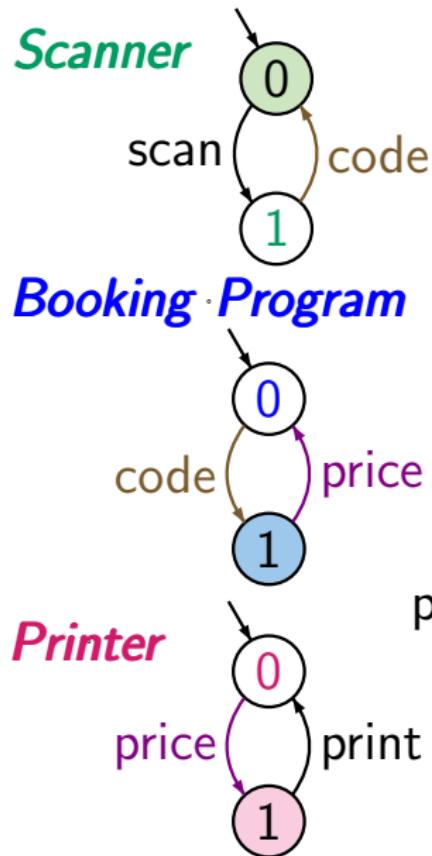
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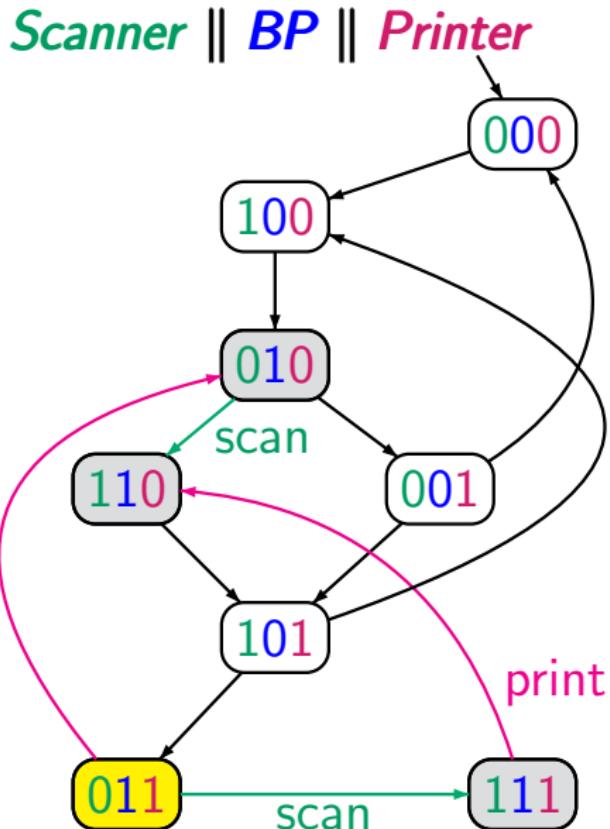
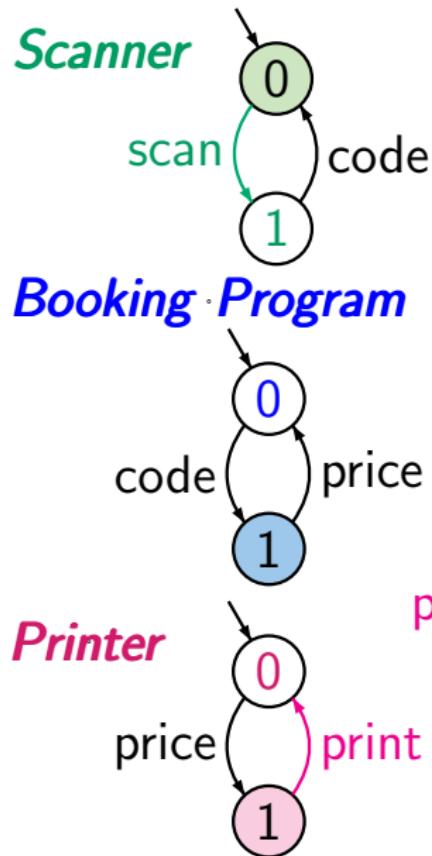
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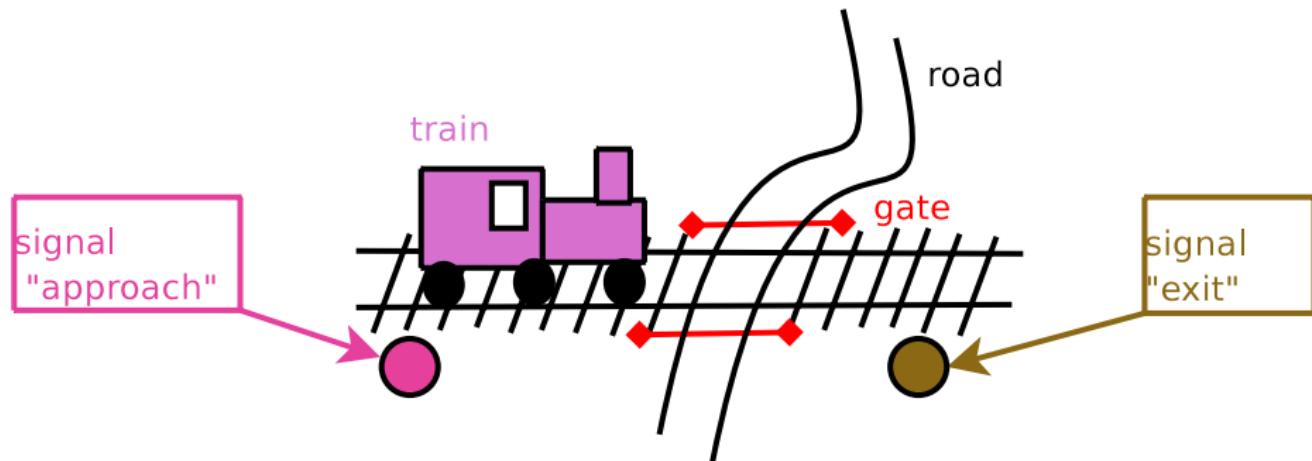
# Interleaving

PC2.2-21



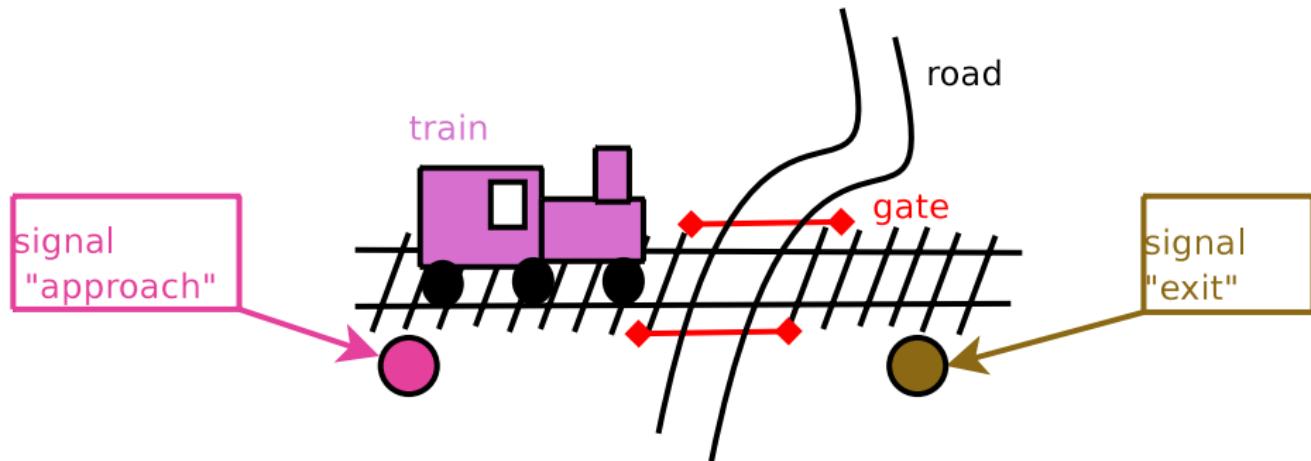
# Railroad crossing

PC2.2-22



# Railroad crossing

PC2.2-22

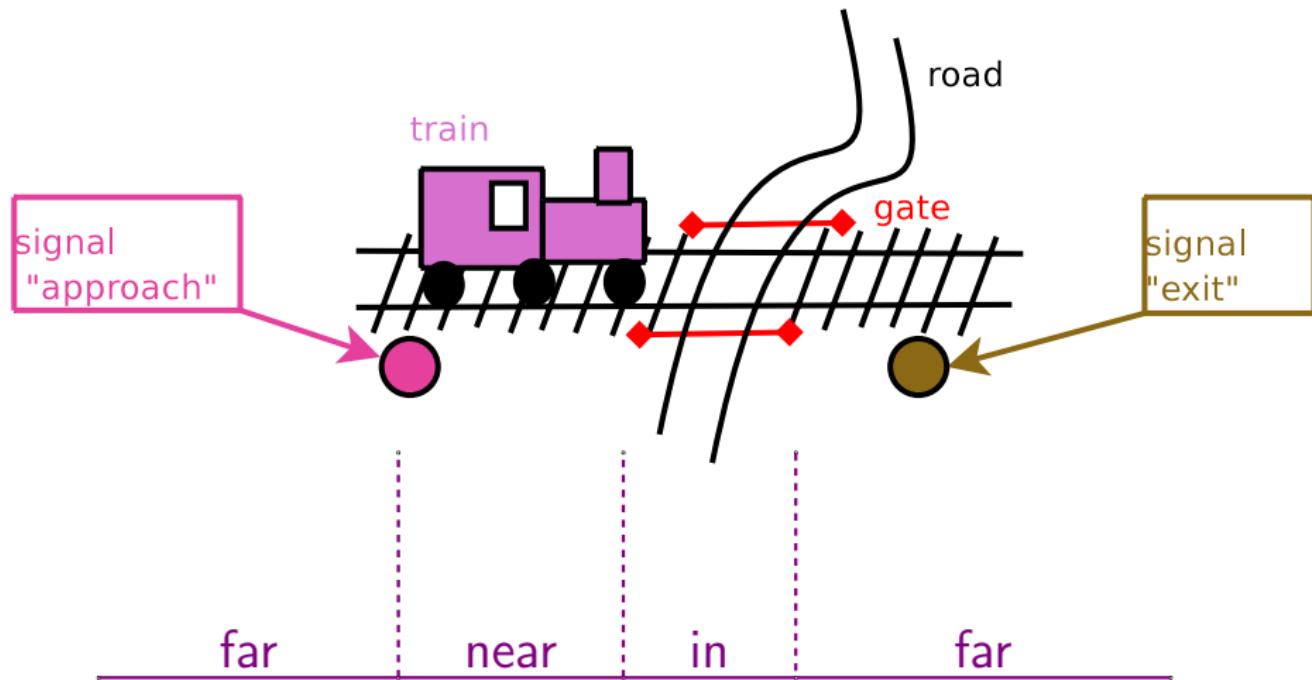


modeling by a transition system with 3 processes:

*Train* || *Controller* || *Gate*

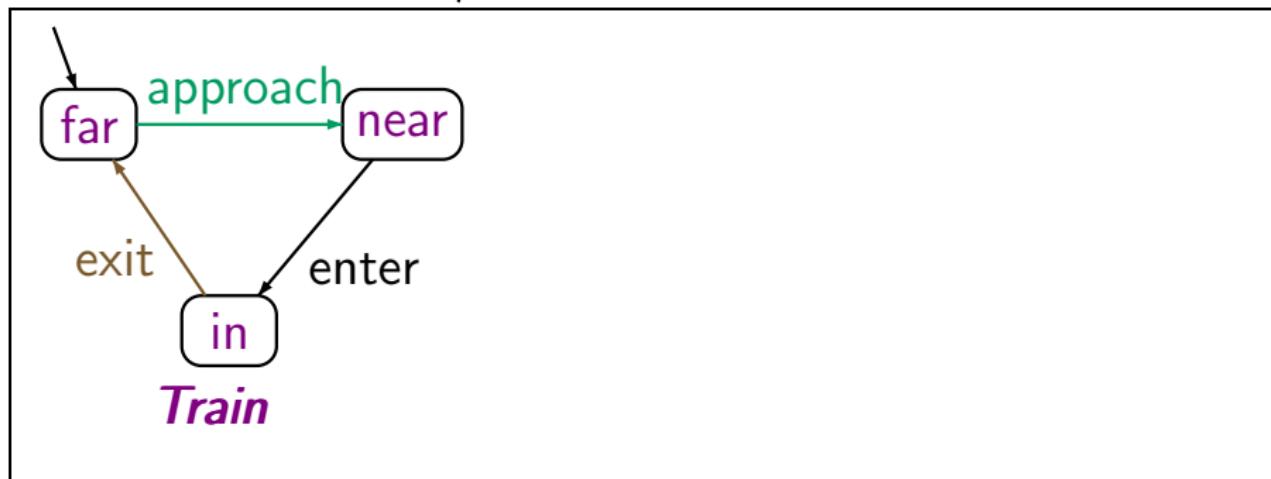
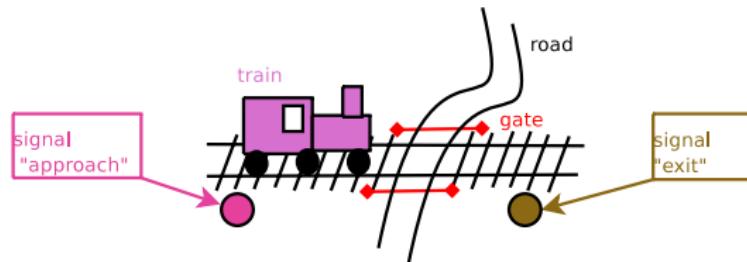
# Modeling the behavior of trains

PC2.2-22



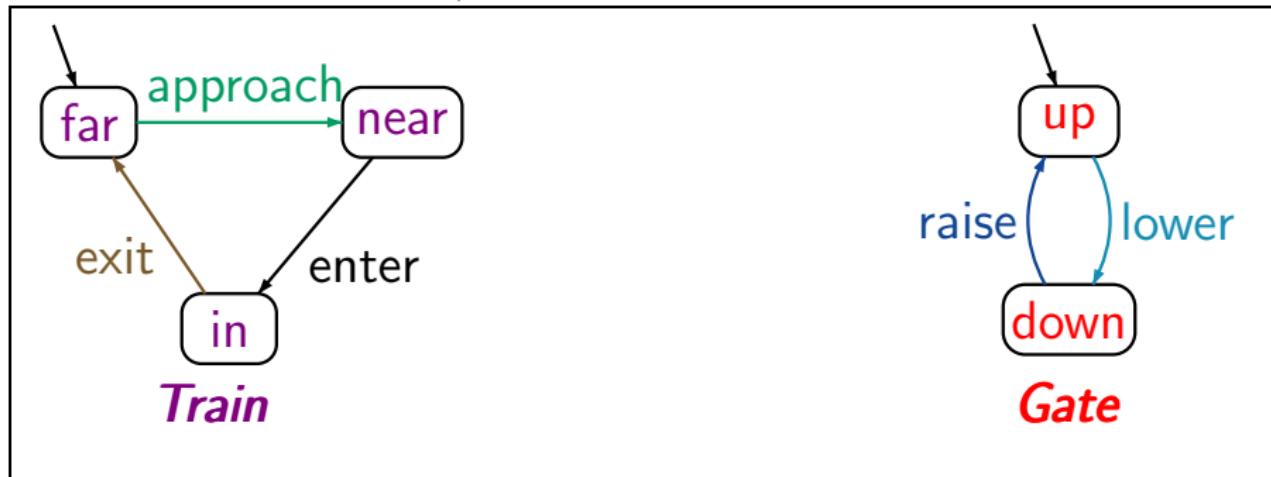
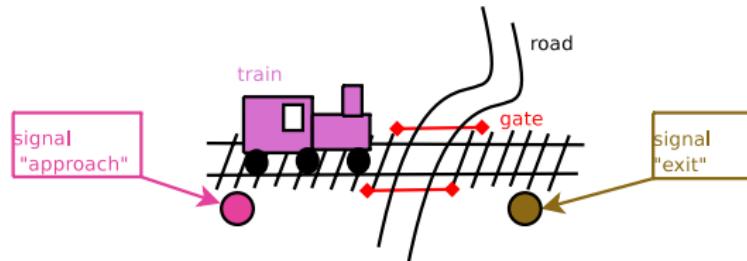
# TS for the trains

PC2.2-22



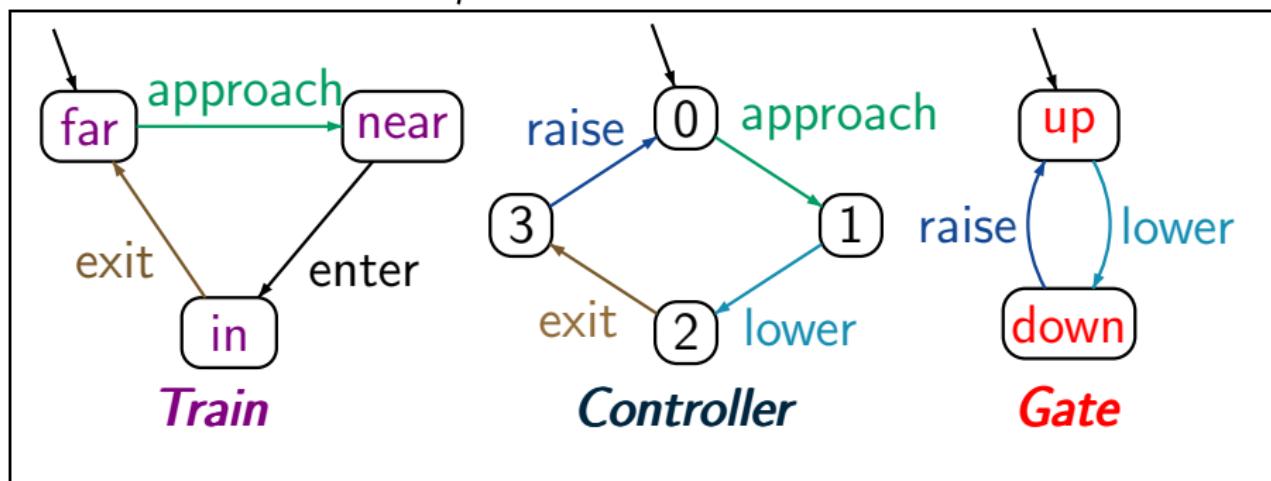
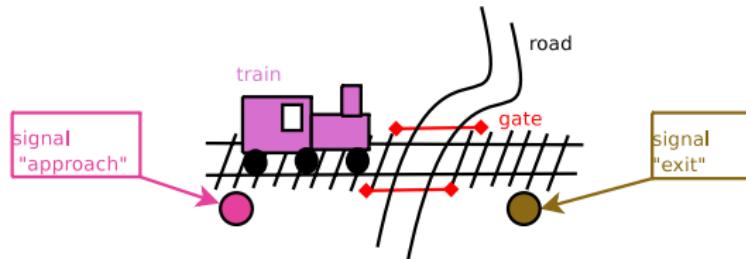
# TS for the trains and gate

PC2.2-22



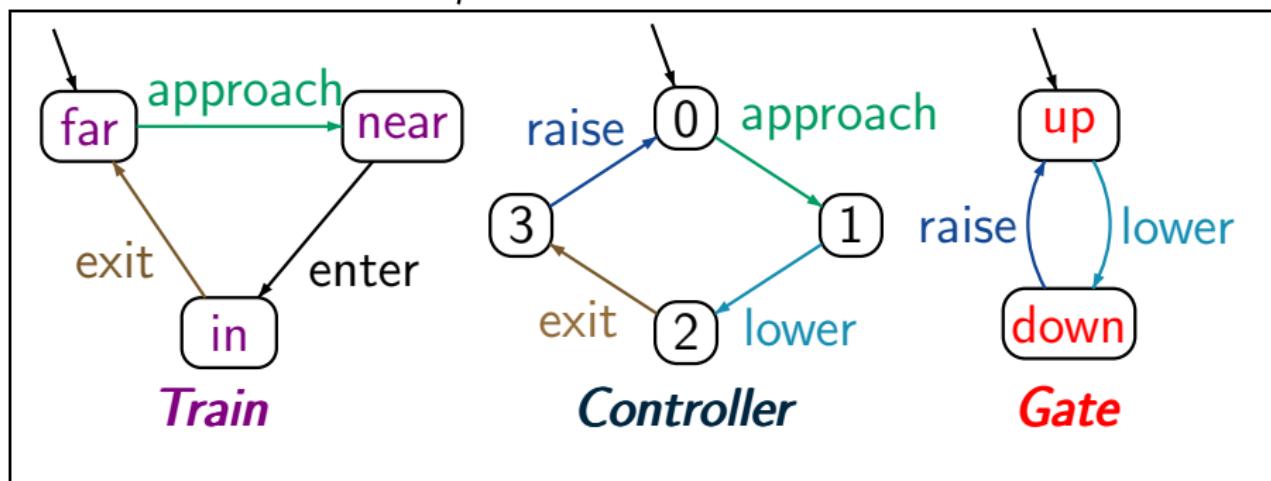
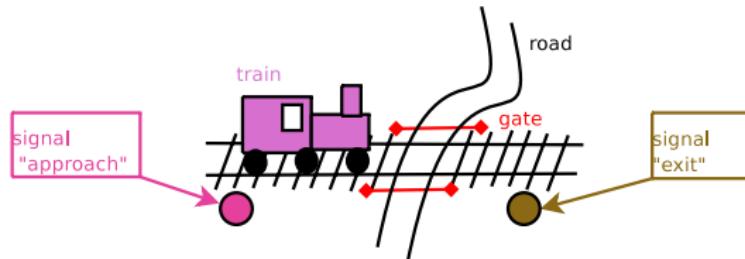
# TS for the trains, controller and gate

PC2.2-22



# TS for the trains, controller and gate

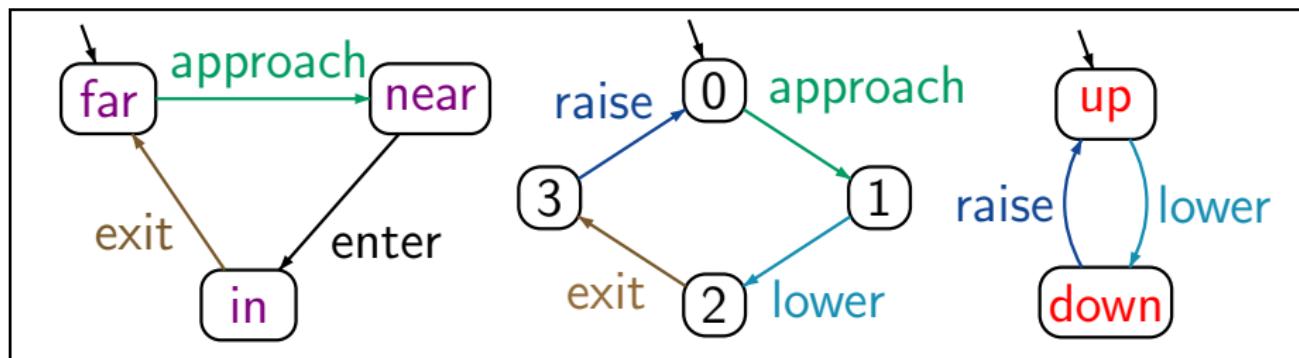
PC2.2-22



transition system *Train* || *Controller* || *Gate*

# TS for railroad crossing

PC2.2-23

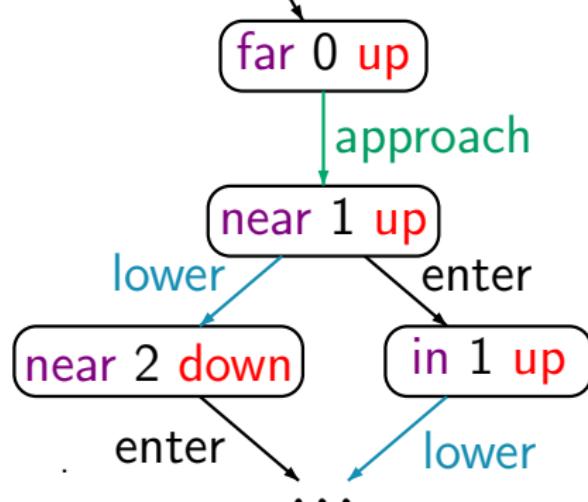
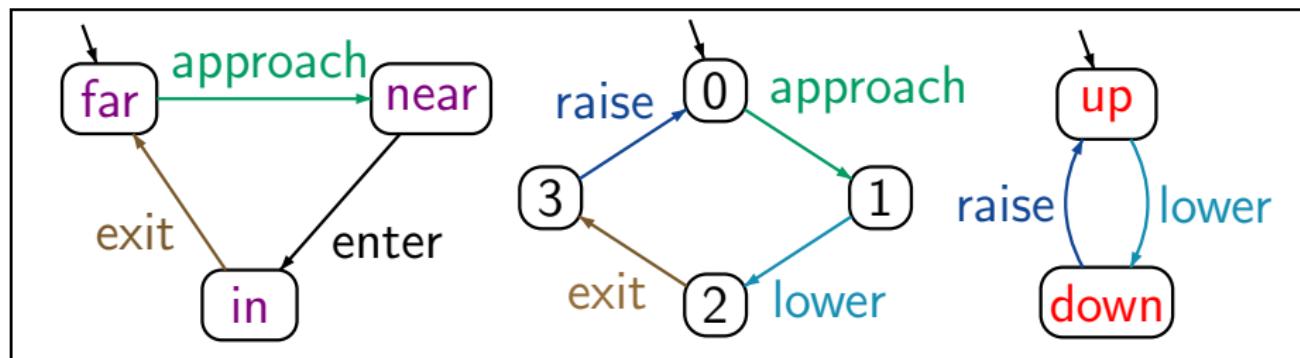


reachable fragment  
of the transition system

***Train*** || ***Controller*** || ***Gate***

# TS for railroad crossing

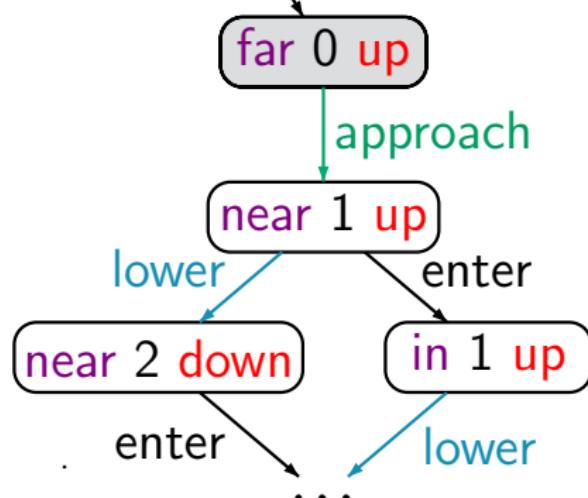
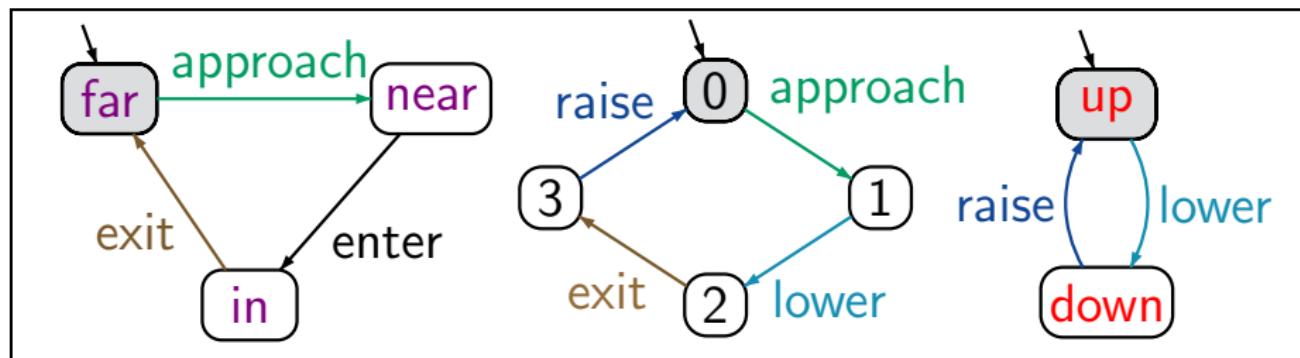
PC2.2-23



reachable fragment  
of the transition system  
***Train* || *Controller* || *Gate***

# TS for railroad crossing

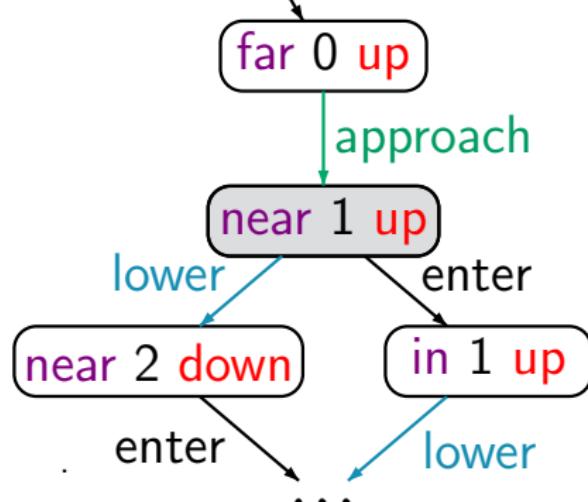
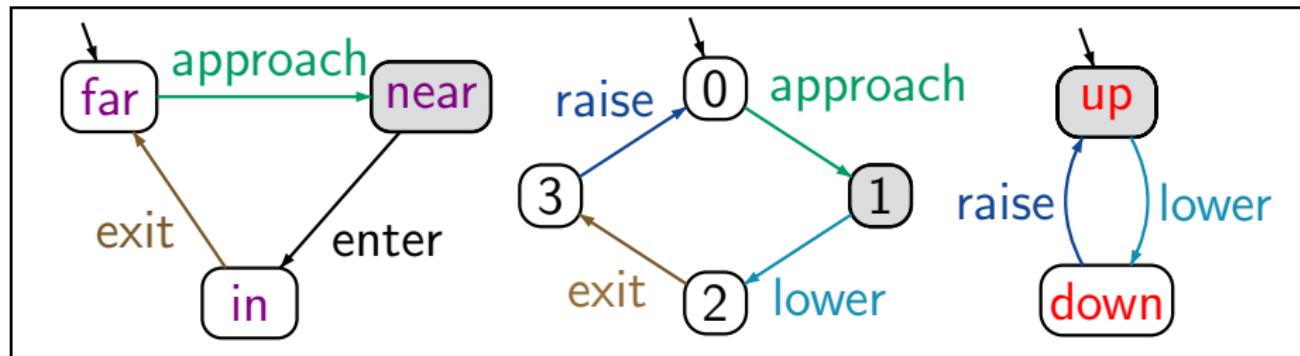
PC2.2-23



reachable fragment  
of the transition system  
***Train* || *Controller* || *Gate***

# TS for railroad crossing

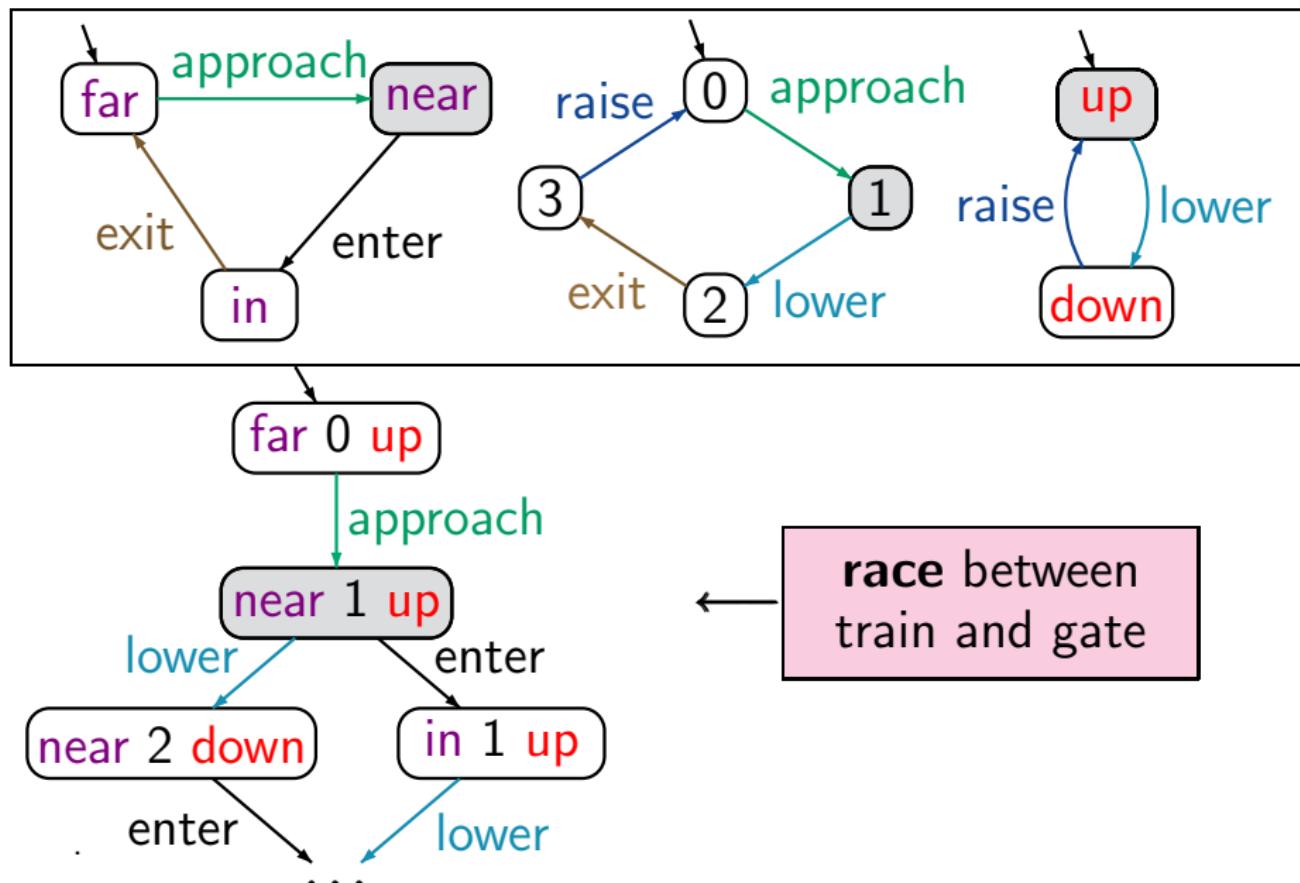
PC2.2-23



reachable fragment  
of the transition system  
*Train* || *Controller* || *Gate*

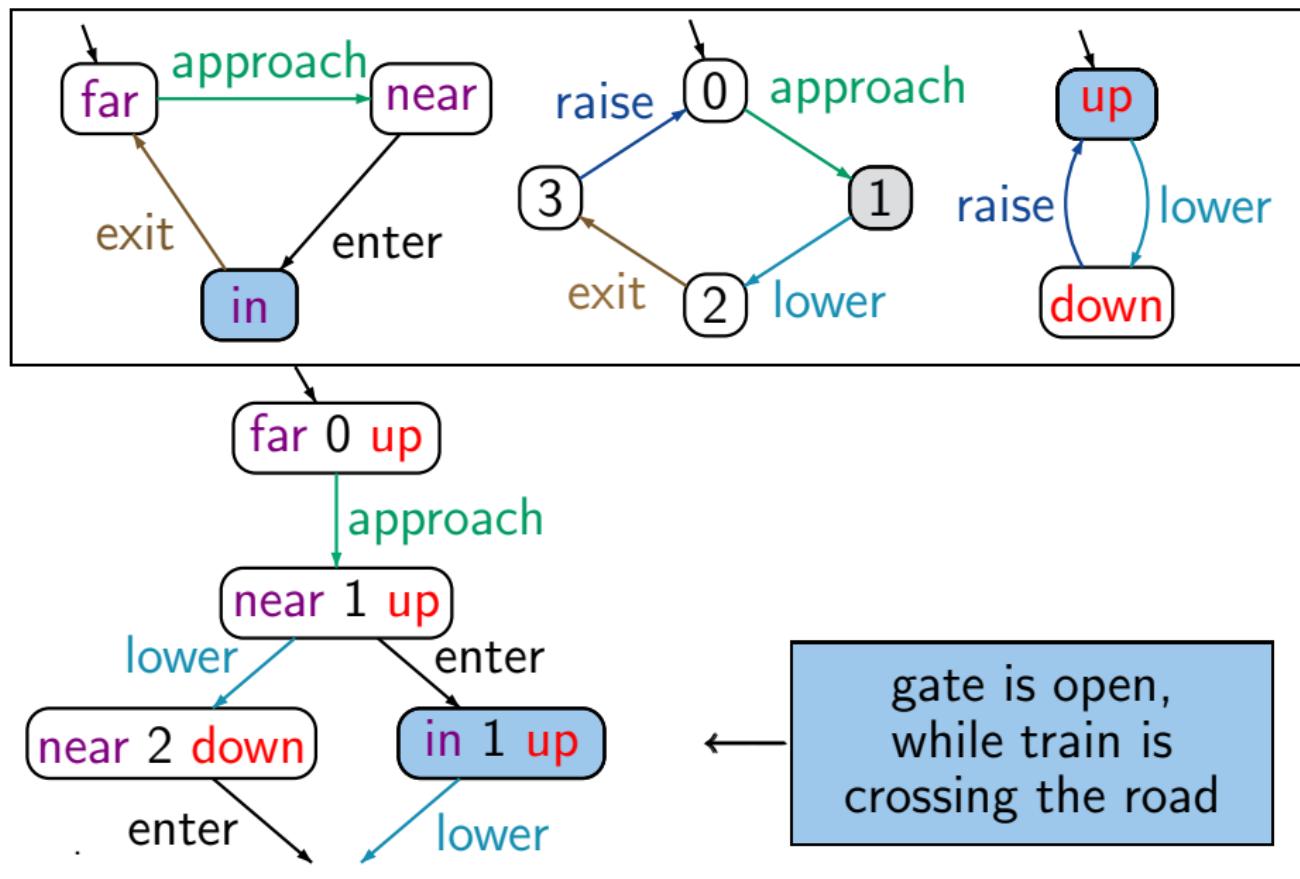
# TS for railroad crossing

PC2.2-23



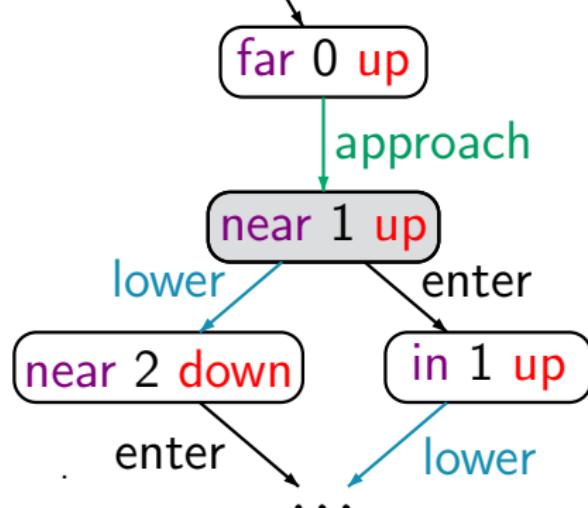
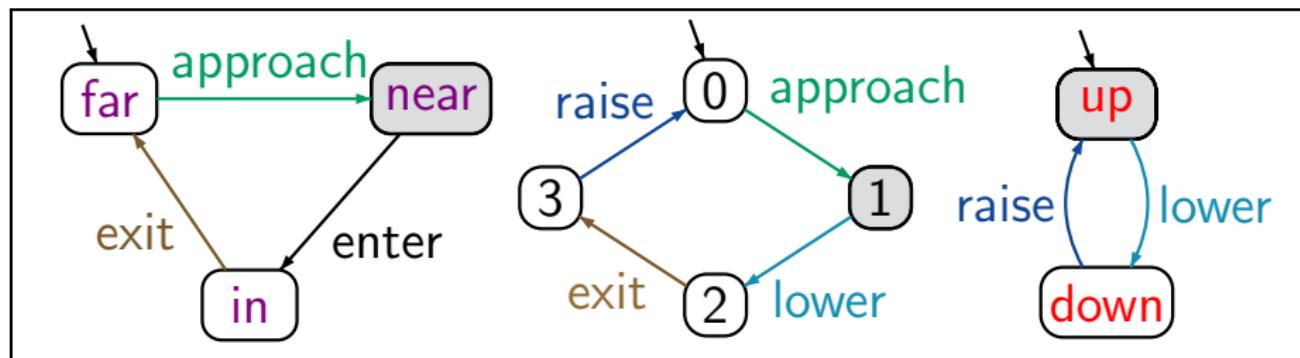
# TS for railroad crossing

PC2.2-23



# TS for railroad crossing

PC2.2-23



← interleaving is time-abstract