

Real-time and Probabilistic Systems Verification

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Topics

- TCTL
- Model Checking for TCTL

More:

The slides in the following pages are taken from the material of the course “Advanced Model Checking” held by Prof. Dr. Ir. Joost-Pieter Katoen at Aachen University.

Timed CTL

Syntax of TCTL *state-formulas* over AP and set C :

$$\Phi ::= \text{true} \mid a \mid g \mid \Phi \wedge \Phi \mid \neg \Phi \mid \exists \varphi \mid \forall \varphi$$

where $a \in AP$, $g \in ACC(C)$ and φ is a *path-formula* defined by:

$$\varphi ::= \Phi U^J \Phi$$

where $J \subseteq \mathbb{R}_{\geq 0}$ is an interval whose bounds are naturals

abbreviate $[c, \infty)$ by $x > c$, $(c_1, c_2]$ by $c_1 < x \leq c_2$ etc.

Some abbreviations

“Always” is obtained in the following way:

$$\exists \square^J \Phi = \neg \forall \diamond^J \neg \Phi \quad \text{and} \quad \forall \square^J \Phi = \neg \exists \diamond^J \neg \Phi$$

$\exists \square^J \Phi$ asserts that for some path during the interval J , Φ holds

$\forall \square^J \Phi$ requires this to hold for all paths

Standard \square and \diamond -operator are obtained as follows:

$$\diamond \Phi = \diamond^{[0, \infty)} \Phi \quad \text{and} \quad \square \Phi = \square^{[0, \infty)} \Phi$$

Semantics of TCTL

For state $s = \langle \ell, \eta \rangle$ in $TS(TA)$ the satisfaction relation \models is defined by:

$$s \models \text{true}$$

$$s \models a \quad \text{iff} \quad a \in L(\ell)$$

$$s \models g \quad \text{iff} \quad \eta \models g$$

$$s \models \neg \Phi \quad \text{iff} \quad \text{not } s \models \Phi$$

$$s \models \Phi \wedge \Psi \quad \text{iff} \quad (s \models \Phi) \text{ and } (s \models \Psi)$$

$$s \models \exists \varphi \quad \text{iff} \quad \pi \models \varphi \text{ for some } \pi \in \text{Paths}_{div}(s)$$

$$s \models \forall \varphi \quad \text{iff} \quad \pi \models \varphi \text{ for all } \pi \in \text{Paths}_{div}(s)$$

path quantification over time-divergent paths only

The \Longrightarrow relation

For infinite path fragments in $TS(TA)$ performing ∞ many actions let:

$$s_0 \xrightarrow{d_0} s_1 \xrightarrow{d_1} s_2 \xrightarrow{d_2} \dots \quad \text{with } d_0, d_1, d_2 \dots \geq 0$$

denote the equivalence class containing all infinite path fragments induced by execution fragments of the form:

$$s_0 \underbrace{\xrightarrow{d_0^1} \dots \xrightarrow{d_0^{k_0}}}_{\substack{\text{time passage of} \\ d_0 \text{ time-units}}} s_0 + d_0 \xrightarrow{\alpha_1} s_1 \underbrace{\xrightarrow{d_1^1} \dots \xrightarrow{d_1^{k_1}}}_{\substack{\text{time passage of} \\ d_1 \text{ time-units}}} s_1 + d_1 \xrightarrow{\alpha_2} s_2 \underbrace{\xrightarrow{d_2^1} \dots \xrightarrow{d_2^{k_2}}}_{\substack{\text{time passage of} \\ d_2 \text{ time-units}}} s_2 + d_2 \xrightarrow{\alpha_3} \dots$$

where $k_i \in \mathbb{N}$, $d_i \in \mathbb{R}_{\geq 0}$ and $\alpha_i \in Act$ such that $\sum_{j=1}^{k_i} d_i^j = d_i$.

For $\pi \in s_0 \xrightarrow{d_0} s_1 \xrightarrow{d_1} \dots$ we have $ExecTime(\pi) = \sum_{i \geq 0} d_i$

Semantics of TCTL

For time-divergent path $\pi \in s_0 \xrightarrow{d_0} s_1 \xrightarrow{d_1} \dots$, we have:

$\pi \models \diamond^J \Psi$ iff $\exists i \geq 0. s_i + d \models \Psi$ for some $d \in [0, d_i]$ with

$$\sum_{k=0}^{i-1} d_k + d \in J \quad \text{and}$$

where for $s_i = \langle \ell_i, \eta_i \rangle$ and $d \geq 0$ we have $s_i + d = \langle \ell_i, \eta_i + d \rangle$

TCTL-semantics for timed automata

- Let TA be a timed automaton with clocks C and locations Loc
- For TCTL-state-formula Φ , the *satisfaction set* $Sat(\Phi)$ is defined by:

$$Sat(\Phi) = \{ s \in Loc \times Eval(C) \mid s \models \Phi \}$$

- TA satisfies TCTL-formula Φ iff Φ holds in all initial states of TA :

$$TA \models \Phi \quad \text{if and only if} \quad \forall l_0 \in Loc_0. \langle l_0, \eta_0 \rangle \models \Phi$$

where $\eta_0(x) = 0$ for all $x \in C$

Characterizing timelock

- TCTL semantics is also well-defined for TA with timelock
- A state contains a timelock whenever no time-divergent paths emanate from it
- A state is *timelock-free* if and only if it satisfies $\exists\Box\text{true}$
 - some time-divergent path satisfies $\Box\text{true}$, i.e., there is ≥ 1 time-divergent path
 - note: for fair CTL, the states in which a fair path starts also satisfy $\exists\Box\text{true}$
- TA is timelock-free iff $\forall s \in \text{Reach}(TS(TA)): s \models \exists\Box\text{true}$
- Timelocks can thus be checked by a timed CTL formula

TCTL model checking

- TCTL model-checking problem: $TA \models \Phi$ for non-Zeno TA

$$\underbrace{TA \models \Phi}_{\text{timed automaton}} \quad \text{iff} \quad \underbrace{TS(TA) \models \Phi}_{\text{infinite transition system}}$$

- Idea: consider a finite quotient of $TS(TA)$ wrt. a bisimulation
 - $TS(TA) / \cong$ is a *region* transition system and denoted $RTS(TA)$
 - dependence on Φ is ignored for the moment . . .
- Transform TCTL formula Φ into an “equivalent” CTL-formula $\hat{\Phi}$
- Then: $TA \models_{\text{TCTL}} \Phi$ iff $\underbrace{RTS(TA)}_{\text{finite transition system}} \models_{\text{CTL}} \hat{\Phi}$

Basic recipe of TCTL model checking

Input: timed automaton TA and TCTL formula Φ (both over AP and C)

Output: $TA \models \Phi$

$\widehat{\Phi} :=$ eliminate the timing parameters from Φ ;

determine the equivalence classes under \cong ;

construct the region transition system $TS = RTS(TA)$;

apply the CTL model-checking algorithm to check $TS \models \widehat{\Phi}$;

$TA \models \Phi$ if and only if $TS \models \widehat{\Phi}$

how does clock equivalence look like?

Eliminating timing parameters

- Eliminate all intervals $J \neq [0, \infty)$ from TCTL formulas
 - introduce a fresh clock, z say, that does not occur in TA
- Formally: for any state s of $TS(TA)$ it holds:

$$s \models \exists \diamond^J \Phi \quad \text{iff} \quad \underbrace{s\{z := 0\}}_{\text{state in } TS(TA \oplus z)} \models \exists \diamond ((z \in J) \wedge \Phi)$$

- where $TA \oplus z$ is TA (over C) extended with $z \notin C$

atomic clock constraints are atomic propositions, i.e., a CTL formula results

Correctness

Let $TA = (Loc, Act, C, \hookrightarrow, Loc_0, Inv, AP, L)$. For clock $z \notin C$, let

$$TA \oplus z = (Loc, Act, C \cup \{z\}, \hookrightarrow, Loc_0, Inv, AP, L).$$

For any state s of $TS(TA)$ it holds that:

$$1. \quad s \models \exists \diamond^J \Psi \quad \text{iff} \quad \underbrace{s\{z := 0\}}_{\text{state in } TS(TA \oplus z)} \models \exists \diamond((z \in J) \wedge \Psi)$$

$$2. \quad s \models \forall \diamond^J \Psi \quad \text{iff} \quad \underbrace{s\{z := 0\}}_{\text{state in } TS(TA \oplus z)} \models \forall \diamond((z \in J) \wedge \Psi)$$

Clock equivalence \cong

(A) Equivalent clock valuations satisfy the same clock constraints g :

$$\eta \cong \eta' \Rightarrow (\eta \models g \text{ iff } \eta' \models g)$$

(B) Time-divergent paths of equivalent states are “equivalent”

– this property guarantees that equivalent states satisfy the same path formulas

(C) The number of equivalence classes under \cong is finite

Clock equivalence

- Correctness criteria (A) and (B) are ensured if equivalent states:
 - agree on the integer parts of all clock values, and
 - agree on the ordering of the fractional parts of all clocks
- ⇒ This yields a denumerable infinite set of equivalence classes
- Observe that:
 - if clocks exceed the maximal constant with which they are compared their precise value is not of interest
- ⇒ The number of equivalence classes is then finite (C)

Clock equivalence: definition

Clock valuations $\eta, \eta' \in \text{Eval}(C)$ are *equivalent*, denoted $\eta \cong \eta'$, if either:

- for all $x \in C$: $\eta(x) > c_x$ iff $\eta'(x) > c_x$, or
- for any $x, y \in C$ with $\eta(x) \leq c_x$ and $\eta(y) \leq c_y$ it holds:
 - $\lfloor \eta(x) \rfloor = \lfloor \eta'(x) \rfloor$ and $\text{frac}(\eta(x)) = 0$ iff $\text{frac}(\eta'(x)) = 0$, and
 - $\text{frac}(\eta(x)) \leq \text{frac}(\eta(y))$ iff $\text{frac}(\eta'(x)) \leq \text{frac}(\eta'(y))$.

$$s \cong s' \quad \text{iff} \quad \ell = \ell' \quad \text{and} \quad \eta \cong \eta'$$

Regions

- The *clock region* of $\eta \in Eval(C)$, denoted $[\eta]$, is defined by:

$$[\eta] = \{ \eta' \in Eval(C) \mid \eta \cong \eta' \}$$

- The *state region* of $s = \langle \ell, \eta \rangle \in TS(TA)$ is defined by:

$$[s] = \langle \ell, [\eta] \rangle = \{ \langle \ell, \eta' \rangle \mid \eta' \in [\eta] \}$$

Bounds on the number of regions

The *number of clock regions* is bounded from below and above by:

$$|C|! * \prod_{x \in C} c_x \leq \underbrace{\left| \text{Eval}(C) / \cong \right|}_{\text{number of regions}} \leq |C|! * 2^{|C|-1} * \prod_{x \in C} (2c_x + 2)$$

where for the upper bound it is assumed that $c_x \geq 1$ for any $x \in C$

the number of state regions is $|Loc|$ times larger

Preservation of atomic properties

1. For $\eta, \eta' \in Eval(C)$ such that $\eta \cong \eta'$:

$$\eta \models g \quad \text{if and only if} \quad \eta' \models g \quad \text{for any } g \in ACC(TA \cup \Phi)$$

2. For $s, s' \in TS(TA)$ such that $s \cong s'$:

$$s \models a \quad \text{if and only if} \quad s' \models a \quad \text{for any } a \in AP'$$

where AP' includes all propositions in TA and atomic clock constraints in TA and Φ

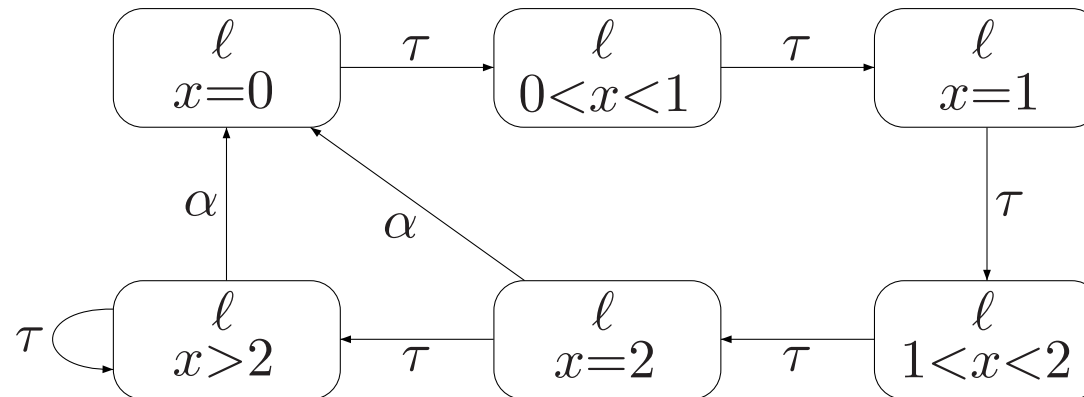
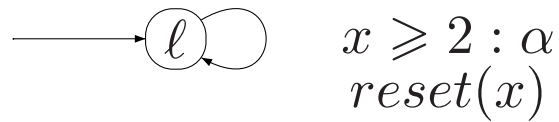
Clock equivalence is a bisimulation

Clock equivalence is a bisimulation equivalence over AP'

Region automaton: intuition

- Region automaton = quotient of $TS(TA)$ under \cong
- State regions are states in quotient transition system under \cong
- Transitions in region automaton “mimic” those in $TS(TA)$
- Delays are **abstract**
 - the exact delay is not recorded, only that some delay took place
 - if any clock x exceeds c_x , delays are self-loops
- Discrete transitions correspond to **actions**

A simple example



Unbounded and successor regions

- Clock region $r_\infty = \{ \eta \in Eval(C) \mid \forall x \in C. \eta(x) > c_x \}$ is *unbounded*
- r' is the *successor (clock) region* of r , denoted $r' = succ(r)$, if either:
 1. $r = r_\infty$ and $r = r'$, or
 2. $r \neq r_\infty$, $r \neq r'$ and $\forall \eta \in r$:

$$\exists d \in \mathbb{R}_{>0}. (\eta + d \in r' \quad \text{and} \quad \forall 0 \leq d' \leq d. \eta + d' \in r \cup r')$$

- The *successor region*: $succ(\langle \ell, r \rangle) = \langle \ell, succ(r) \rangle$
- Note: the location invariants are ignored so far!

Characterizing time convergence

For non-zero TA and $\pi = s_0 s_1 s_2 \dots$ a path in $TS(TA)$:

(a) π is *time-convergent* $\Rightarrow \exists$ state region $\langle \ell, r \rangle$ such that for some j :

$$s_i \in \langle \ell, r \rangle \text{ for all } i \geq j$$

(b) If \exists state region $\langle \ell, r \rangle$ with $r \neq r_\infty$ and an index j such that:

$$s_i \in \langle \ell, r \rangle \text{ for all } i \geq j$$

then π is *time-convergent*

time-convergent paths are paths that only perform delays from some time instant on

Region automaton

For non-zeno TA with $TS(TA) = (S, Act, \rightarrow, I, AP, L)$ let:

$$RTS(TA, \Phi) = (S', Act \cup \{\tau\}, \rightarrow', I, AP', L') \quad \text{with}$$

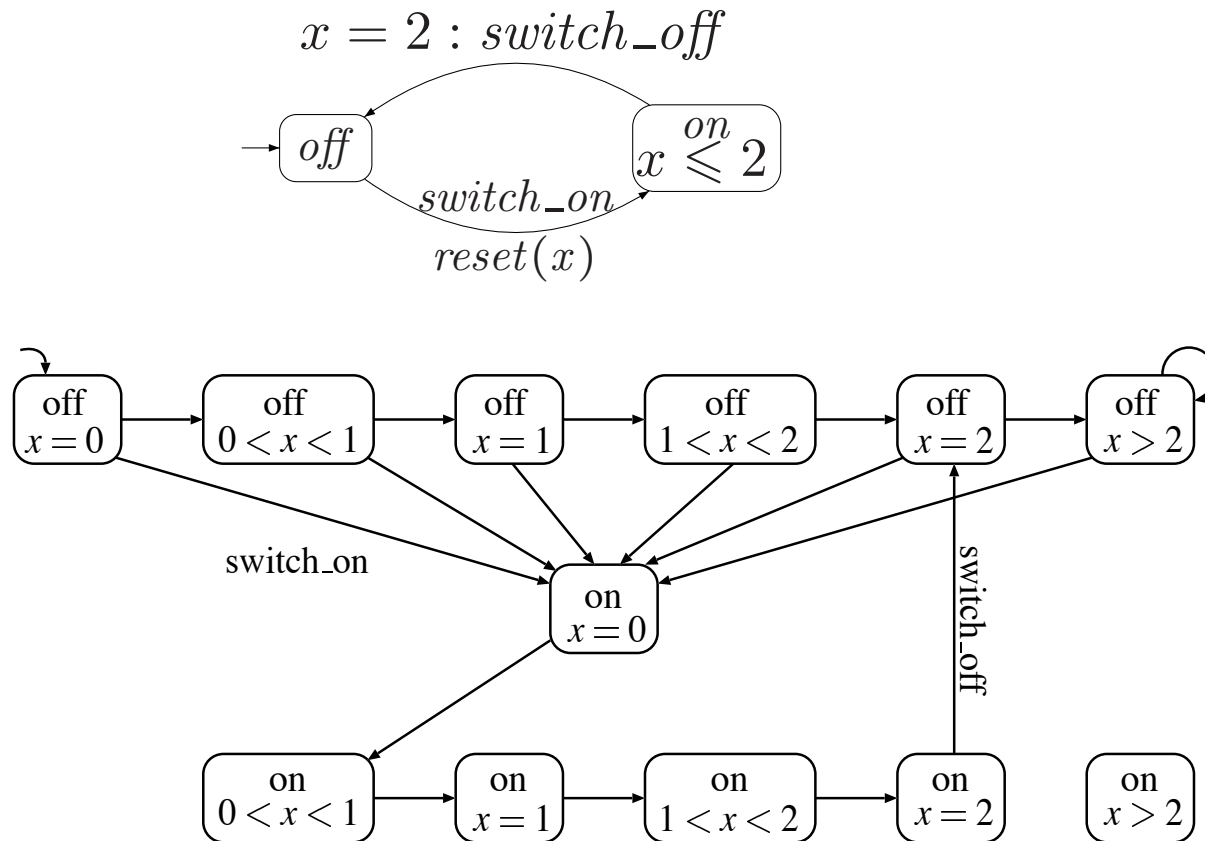
- $S' = S / \cong = \{[s] \mid s \in S\}$ and $I' = \{[s] \mid s \in I\}$, the state regions

- $L'(\langle \ell, r \rangle) = L(\ell) \cup \{g \in AP' \setminus AP \mid r \models g\}$

- \rightarrow' is defined by:
$$\frac{\ell \xrightarrow{g:\alpha,D} l' \quad r \models g \quad \text{reset } D \text{ in } r \models \text{Inv}(l')}{\langle \ell, r \rangle \xrightarrow{\alpha}' \langle l', \text{reset } D \text{ in } r \rangle}$$

and
$$\frac{r \models \text{Inv}(\ell) \quad \text{succ}(r) \models \text{Inv}(\ell)}{\langle \ell, r \rangle \xrightarrow{\tau}' \langle \ell, \text{succ}(r) \rangle}$$

Example: simple light switch



Correctness theorem [Alur and Dill, 1989]

For non-Zeno timed automaton TA and TCTL $_{\diamond}$ formula Φ :

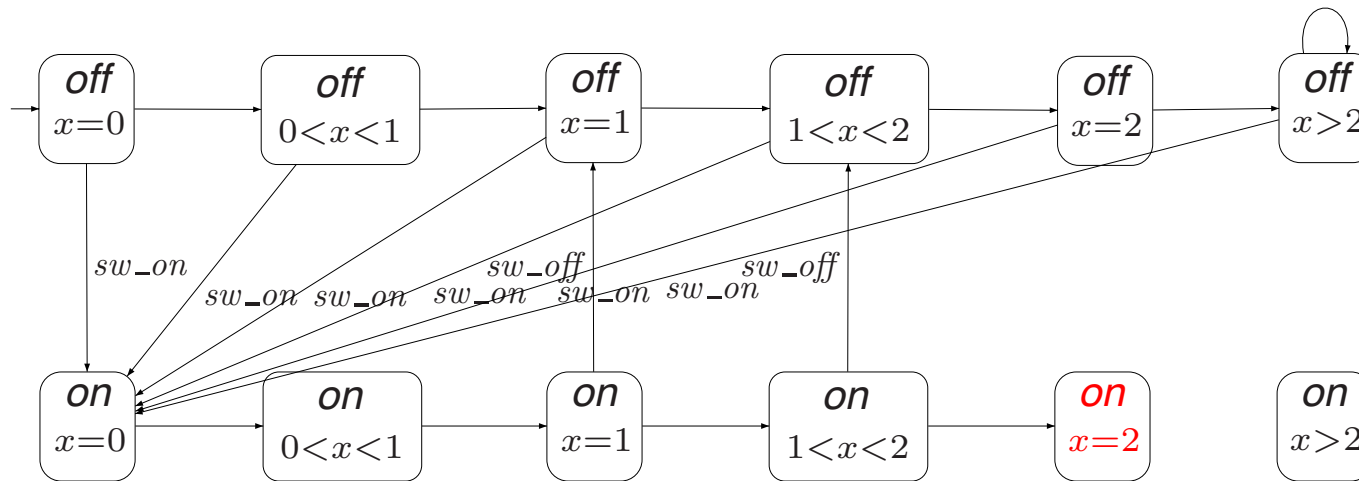
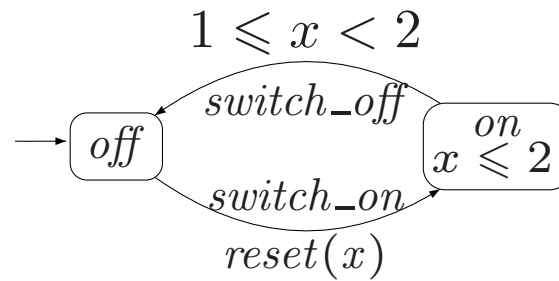
$$\underbrace{TA \models \Phi}_{\text{TCTL semantics}} \quad \text{iff} \quad \underbrace{RTS(TA, \Phi) \models \Phi}_{\text{CTL semantics}}$$

Characterizing timelock freedom

Non-zero TA is timelock-free iff no reachable state in $RTS(TA)$ is terminal

timelocks can thus be checked by a reachability analysis of $RTS(TA)$

Example



Time complexity

For timed automaton TA and $TCTL_{\diamond}$ formula Φ , the model-checking problem

$TA \models \Phi$ can be determined in time $\mathcal{O}((N+K) \cdot |\Phi|)$,

where N and K are the number of states and transitions in $RTS(TA, \Phi)$

Other verification problems

1. The TCTL model-checking problem is **PSPACE-complete**
2. Model checking safety, reachability, or ω -regular properties in TA is **PSPACE-complete**
3. Model checking LTL and CTL against TA is **PSPACE-complete**
4. The model-checking problem for timed LTL is **undecidable**
5. The satisfaction problem for TCTL is **undecidable**

all facts without proof