Memoria Interna

Corso di Architettura degli Elaboratori (teoria)

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Scuola di Scienze e Tecnologie - Sezione di Informatica

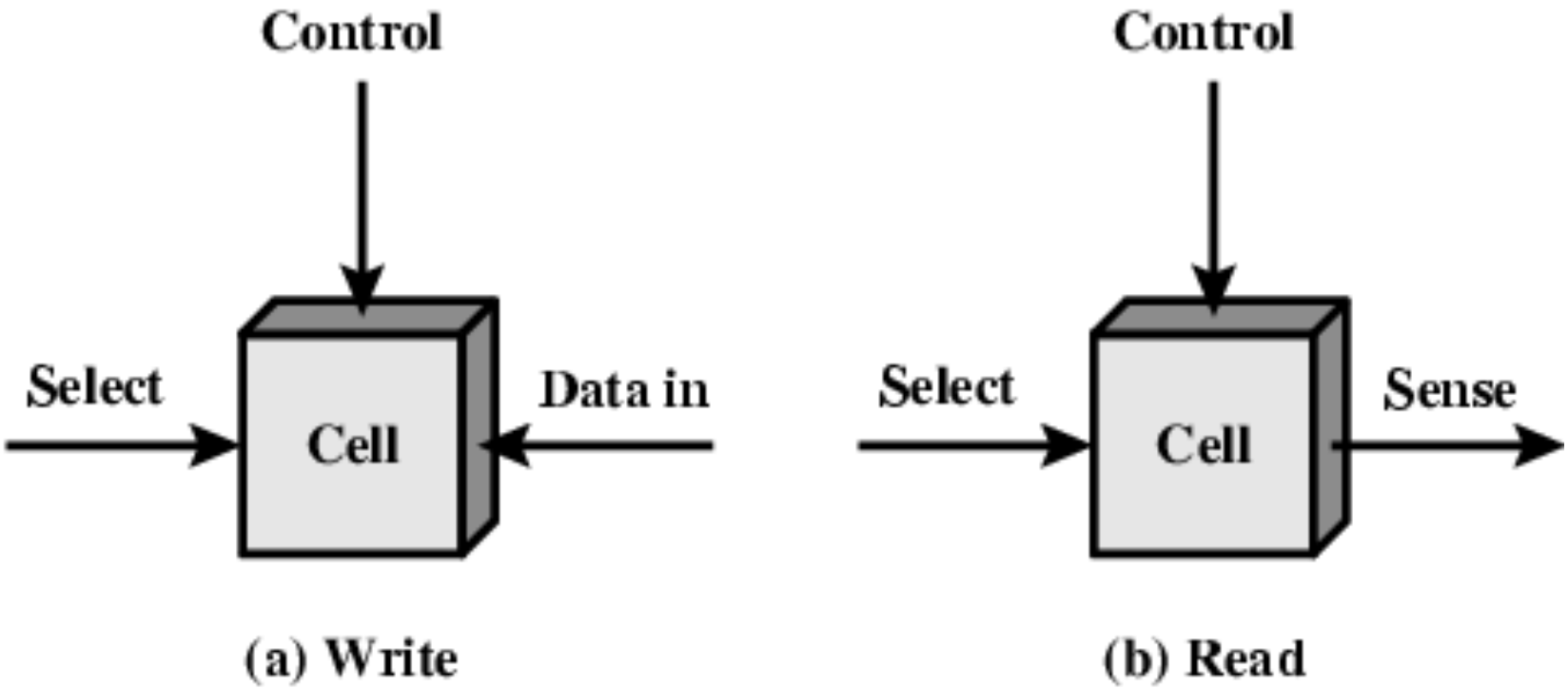
Architettura degli Elaboratori e Laboratorio

William Stallings
Computer Organization and Architecture
8th Edition

Chapter 5

Internal Memory

Memory Cell Operation



Semiconductor Memory Types

<table>
<tr><th>Memory Type</th><th>Category</th><th>Erasure</th><th>Write Mechanism</th><th>Volatility</th></tr>
<tr><td>Random-access memory (RAM)</td><td>Read-write memory</td><td>Electrically, byte-level</td><td>Electrically</td><td>Volatile</td></tr>
<tr><td>Read-only memory (ROM)</td><td rowspan="2">Read-only memory</td><td rowspan="2">Not possible</td><td>Masks</td><td rowspan="6">Nonvolatile</td></tr>
<tr><td>Programmable ROM (PROM)</td><td rowspan="4">Electrically</td></tr>
<tr><td>Erasable PROM (EPROM)</td><td rowspan="3">Read-mostly memory</td><td>UV light, chip-level</td></tr>
<tr><td>Electrically Erasable PROM (EEPROM)</td><td>Electrically, byte-level</td></tr>
<tr><td>Flash memory</td><td>Electrically, block-level</td></tr>
</table>

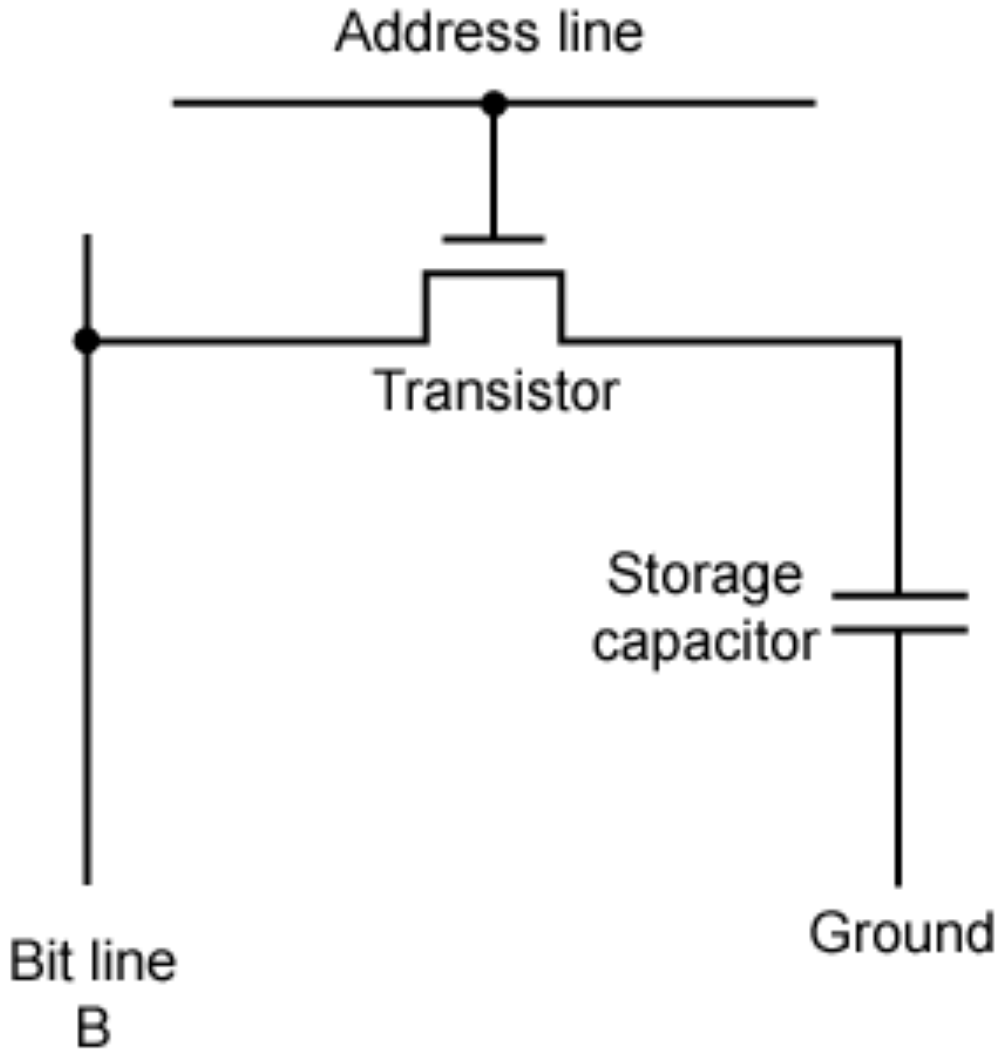
Semiconductor Memory

- RAM
  - Misnamed as all semiconductor memory is random access
  - Read/Write
  - Volatile
  - Temporary storage
  - Static or dynamic

Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Used in main memory
- Essentially analogue
  - —Level of charge determines value

Dynamic RAM Structure



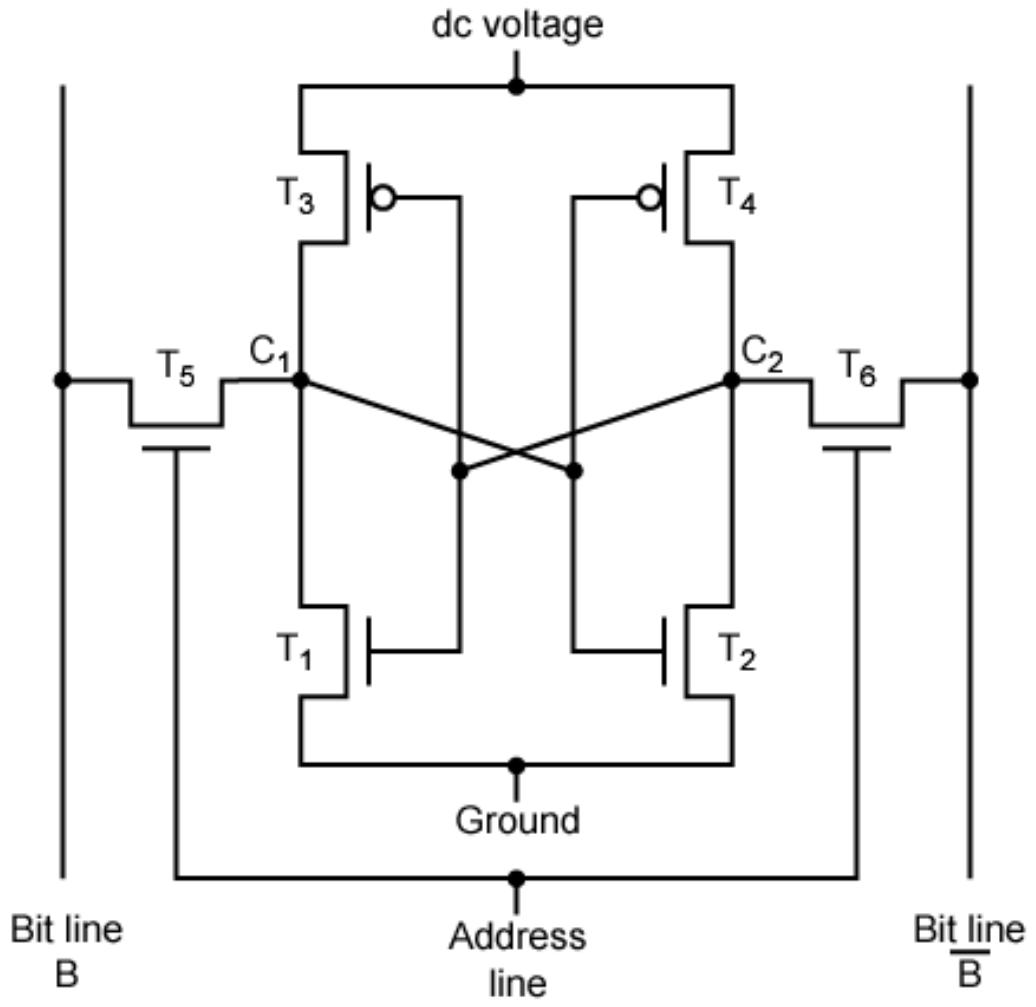
DRAM Operation

- Address line active when bit read or written
  - Transistor switch closed (current flows)
- Write
  - Voltage to bit line
    - High for 1 low for 0
  - Then signal address line
    - Transfers charge to capacitor
- Read
  - Address line selected
    - transistor turns on
  - Charge from capacitor fed via bit line to sense amplifier
    - Compares with reference value to determine 0 or 1
  - Capacitor charge must be restored

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Used in cache
- Digital
  - —Uses flip-flops

Stating RAM Structure



Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6 is switch
- Write – apply value to B & compliment to $\overline{B}$
- Read – value is on line B

SRAM v DRAM

- Both volatile
  - Power needed to preserve data
- Dynamic cell
  - Simpler to build, smaller
  - More dense
  - Less expensive
  - Needs refresh
  - Larger memory units
- Static
  - Faster
  - Cache

Read Only Memory (ROM)

- Permanent storage
  - —Nonvolatile
- Microprogramming (see later)
- Library subroutines
- Systems programs (BIOS)
- Function tables

Types of ROM

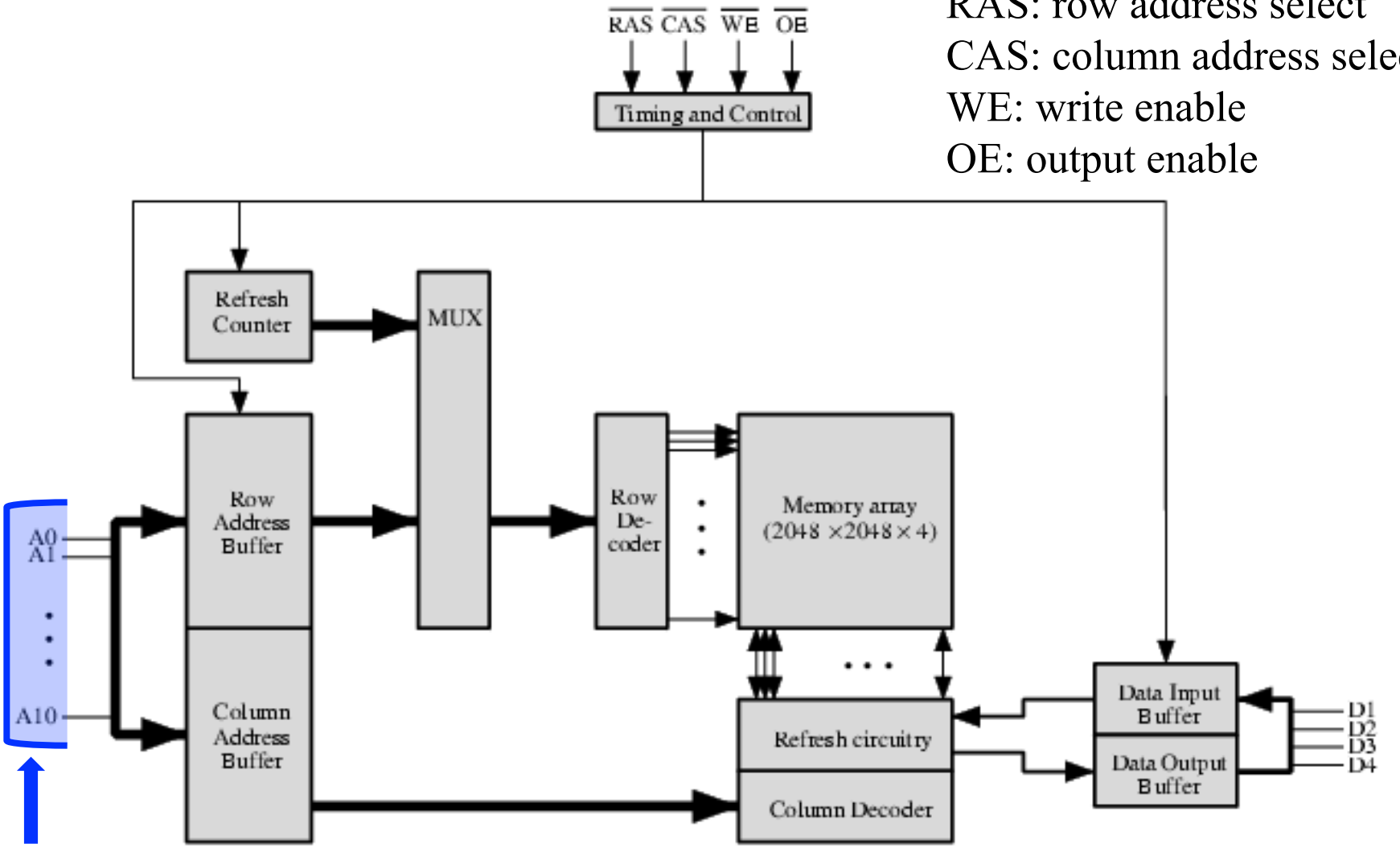
- Written during manufacture
  - Very expensive for small runs
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read “mostly”
  - Erasable Programmable (EPROM)
    - Erased by UV
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
  - Flash memory
    - Erase whole memory electrically

Organisation in detail

- A 16Mbit chip can be organised as 1M of 16 bit words
- A one-bit-per-chip system has 16 chip of 1Mbit storage with bit 1 of each word in chip 1 and so on
- A 16Mbit chip can be organised as a 2048 x 2048 x 4bit array
  - Reduces number of address pins
    - Multiplex row address and column address
    - 11 pins to address (2^{11}=2048)
    - Adding one more pin doubles range of values so x4 capacity

Typical 16 Mb DRAM (4M x 4)

RAS: row address select
CAS: column address select
WE: write enable
OE: output enable



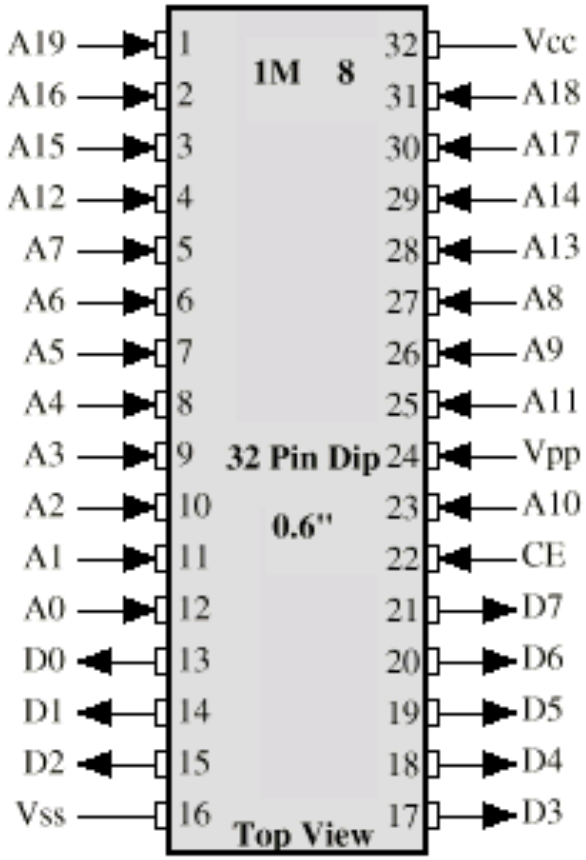
11 bit for addressing

Refreshing

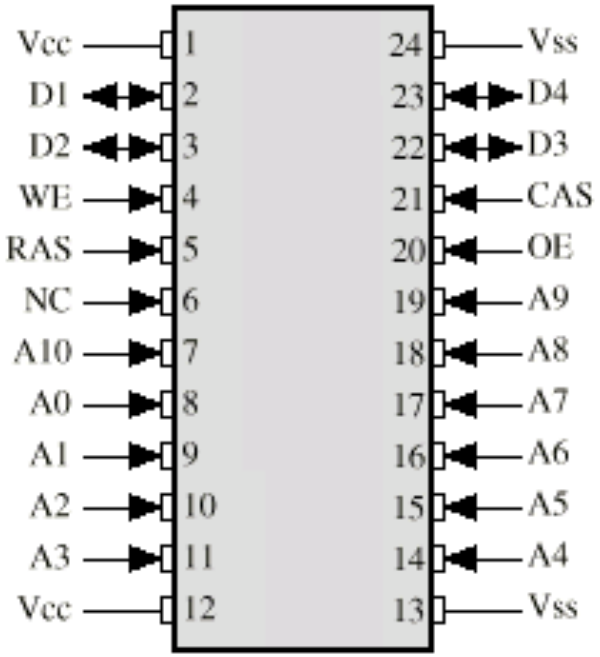
- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

Chip Packaging

8Mbit = 2^{20} x 2^3



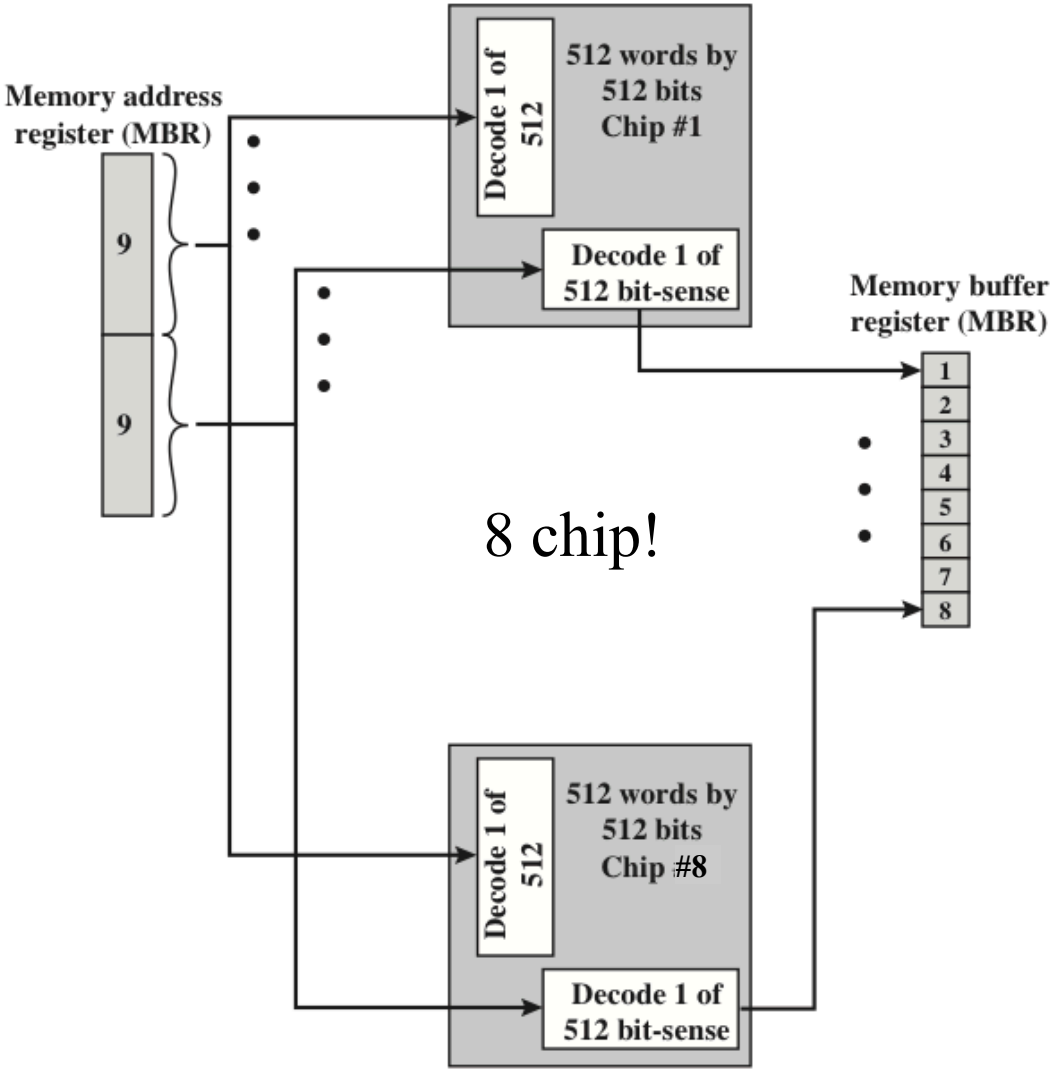
(a) 8 Mbit EPROM



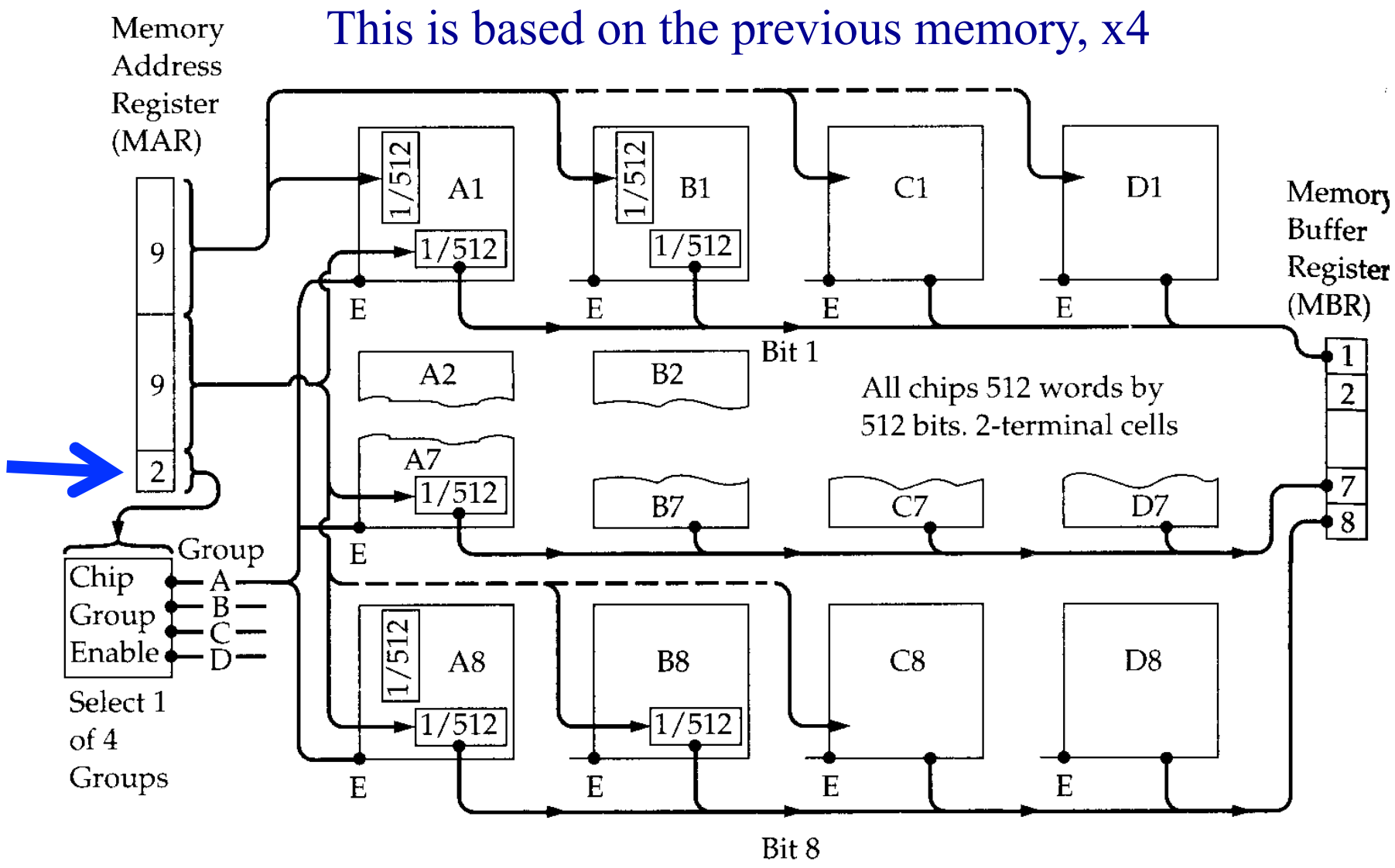
16Mbit=2^{22} x 2^2
addresses are multiplexed

(b) 16 Mbit DRAM

256kByte Module Organisation



1MByte Module Organisation



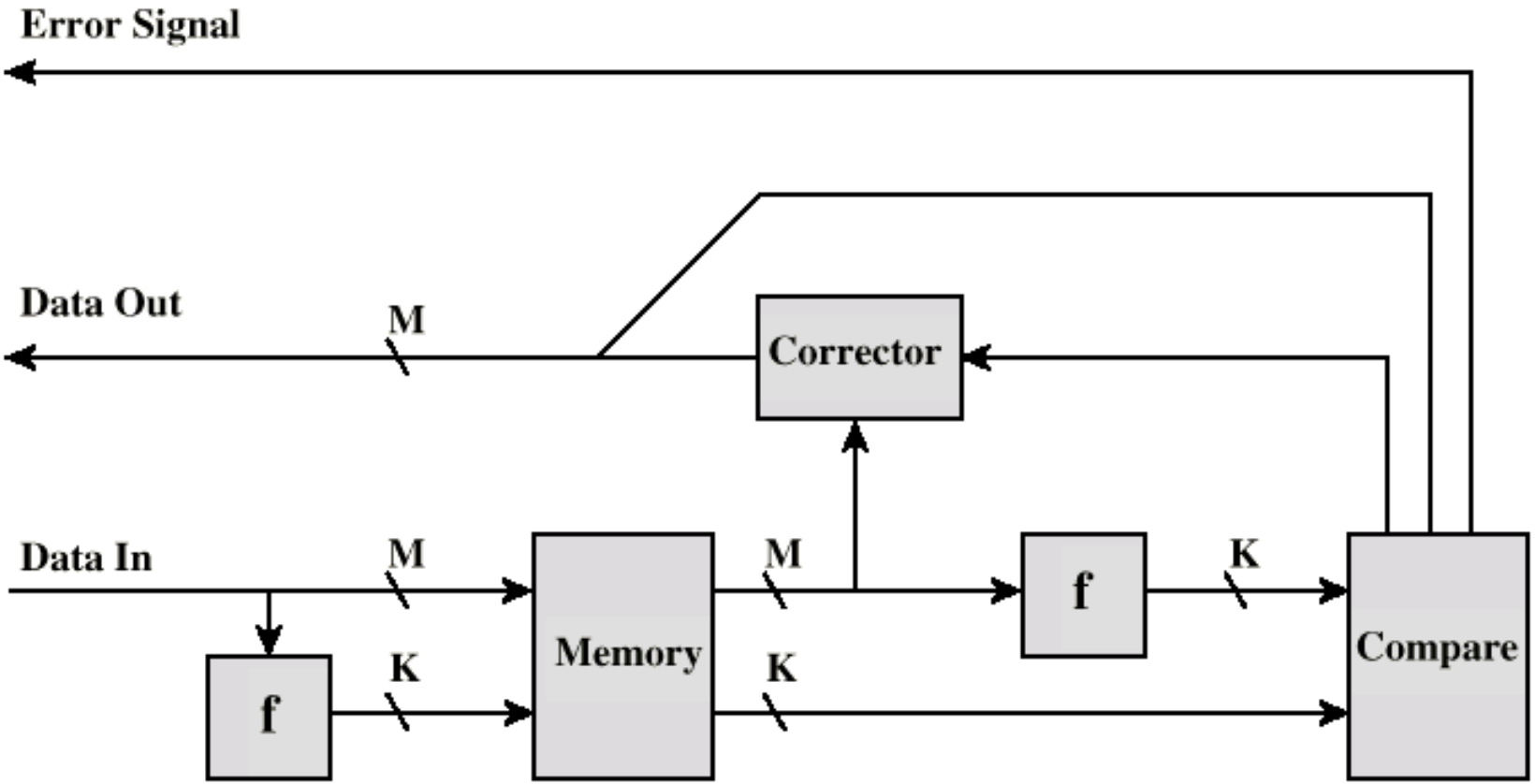
Interleaved Memory

- Collection of DRAM chips
- Grouped into memory bank
- Banks independently service read or write requests
- K banks can service k requests simultaneously

Error Correction

- Hard Failure
  - —Permanent defect
- Soft Error
  - —Random, non-destructive
  - —No permanent damage to memory
- Detected using Hamming error correcting code

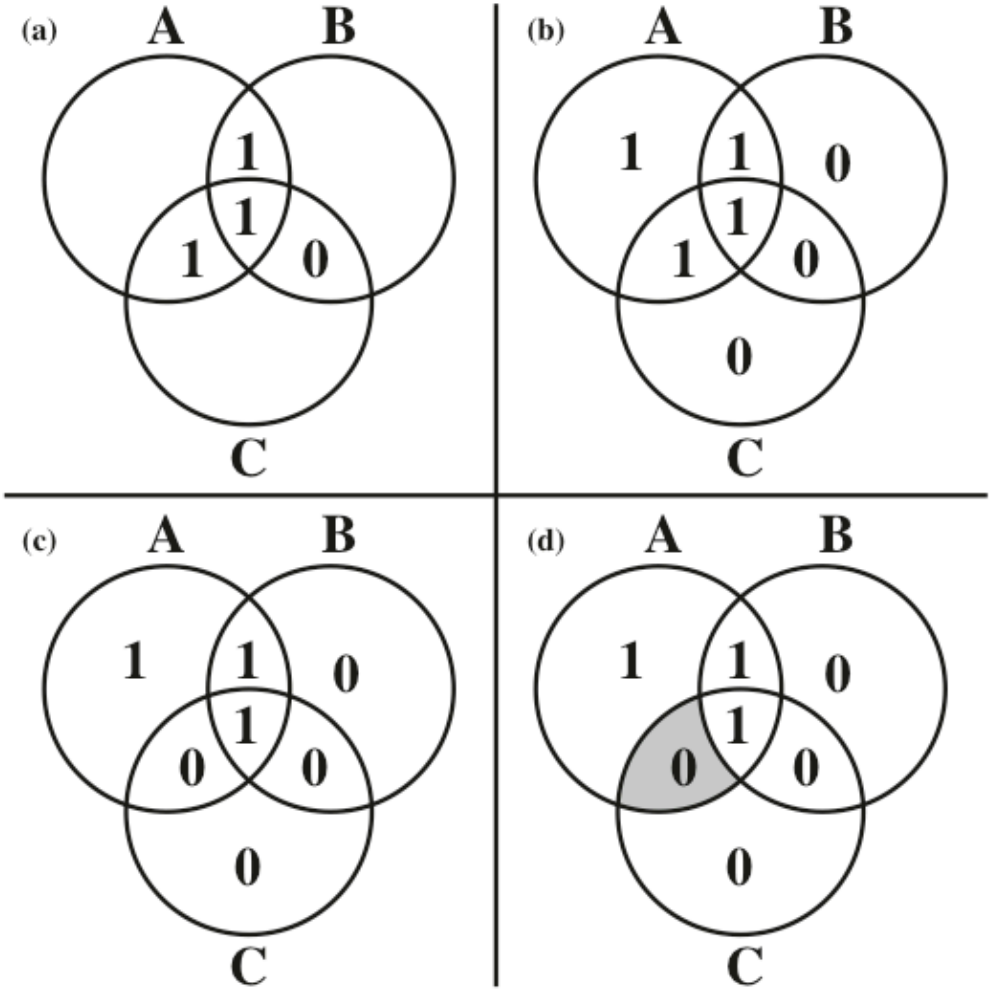
Error Correcting Code Function



Hamming code

- Example using 4 bit for data and 3 for code
- M=4
- K=3

$$2^K-1 \geq M+K$$



Hamming code

Bit Position	12	11	10	9	8	7	6	5	4	3	2	1
Position Number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data Bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check Bit					C8				C4		C2	C1

C1 => D1, D2, D4, D5, D7
C2 => D1, D3, D4, D6, D7
C4 => D2, D3, D4, D8
C8 => D5, D6, D7, D8

To determine the bit controlled by a control bit we should look at the position, not the name of a bit

Hamming code (SEC – single error correcting)

Starting from 8 bit data D1-D8 (from right to left), C8-C4-C2-C1 express parity:

00111001 => C8=0, C4=1, C2=1, C1=1

We assume to have an error in D3

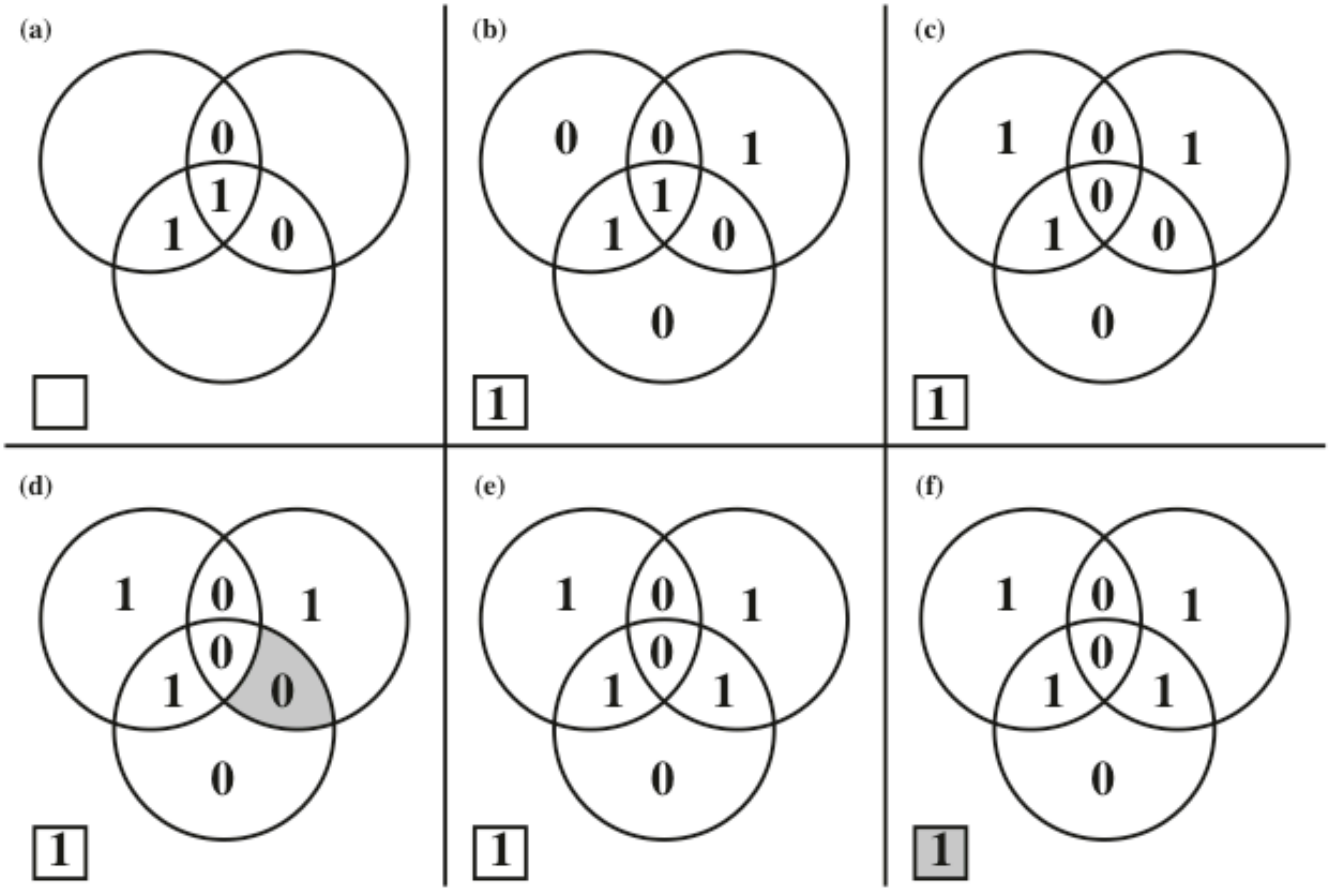
00111100 => C8=0, C4=0, C2=0, C1=1

Parity has changed, a xor op. show where:

0111 xor 0001 = 0110 => 6 => bit in 6° position (starting from right!) =>D3

SEC-DEC (double error detecting)

- 1 bit for the parity of the whole "diagram". This detect an error.



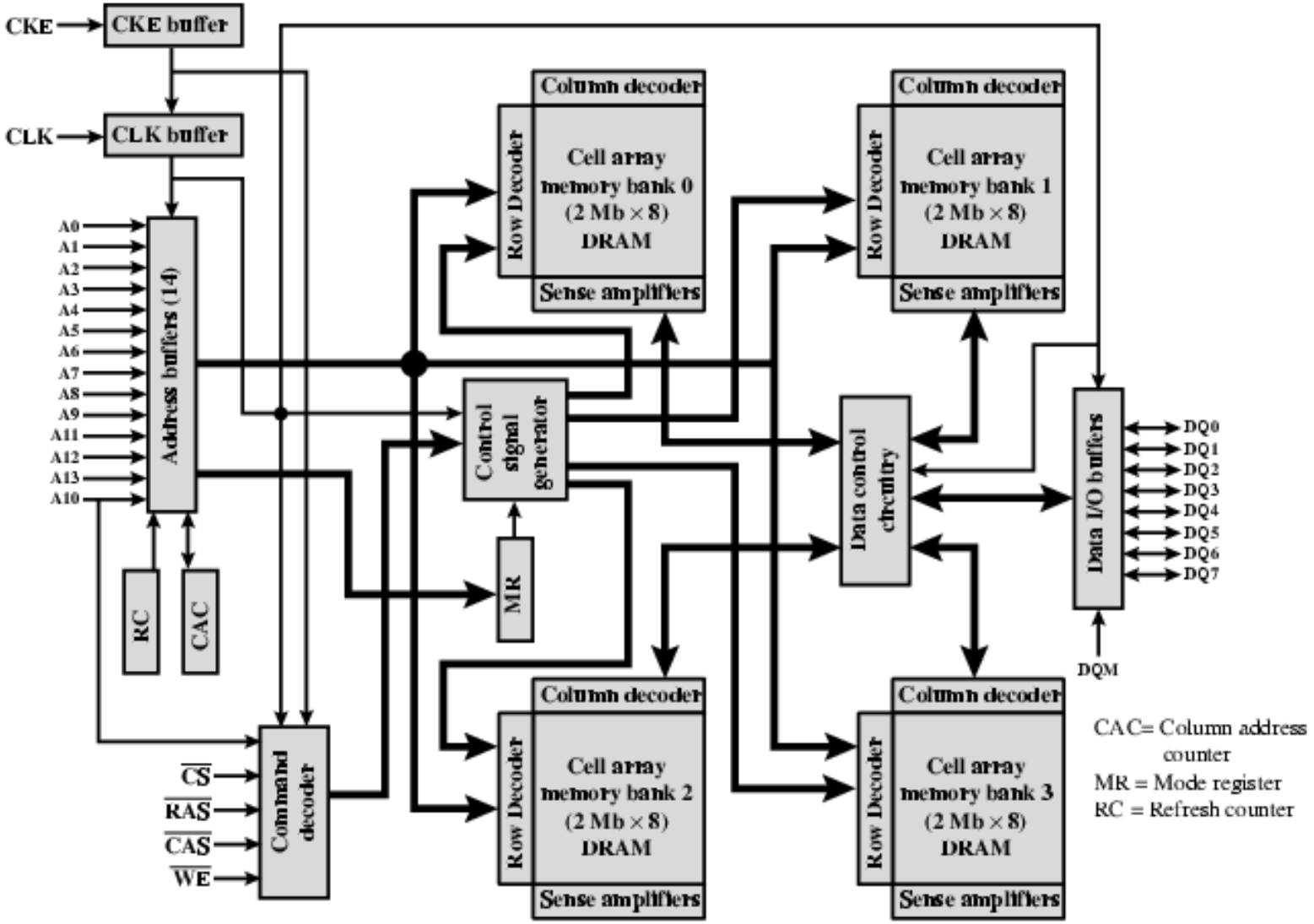
Advanced DRAM Organization

- Basic DRAM same since first RAM chips
- Enhanced DRAM
  - —Contains small SRAM as well
  - —SRAM holds last line read (c.f. Cache!)
- Cache DRAM
  - —Larger SRAM component
  - —Use as cache or serial buffer

Synchronous DRAM (SDRAM)

- Access is synchronized with an external clock
- Address is presented to RAM
- RAM finds data (CPU waits in conventional DRAM)
- Since SDRAM moves data in time with system clock, CPU knows when data will be ready
- CPU does not have to wait, it can do something else
- Burst mode allows SDRAM to set up stream of data and fire it out in block
- DDR-SDRAM sends data twice per clock cycle (leading & trailing edge)

SDRAM


CKE
CKE buffer
CLK
CLK buffer
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A11
A12
A13
A10
Address buffers (14)
RC
CAC
Control signal generator
MR
Column decoder
Row Decoder
Cell array memory bank 0 (2 Mb × 8) DRAM
Sense amplifiers
Column decoder
Row Decoder
Cell array memory bank 1 (2 Mb × 8) DRAM
Sense amplifiers
Data control circuitry
Data I/O buffers
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQM
Column decoder
Row Decoder
Cell array memory bank 2 (2 Mb × 8) DRAM
Sense amplifiers
Column decoder
Row Decoder
Cell array memory bank 3 (2 Mb × 8) DRAM
Sense amplifiers
CS
RAS
CAS
WE
Command decoder
CAC= Column address counter
MR = Mode register
RC = Refresh counter

SDRAM Read Timing

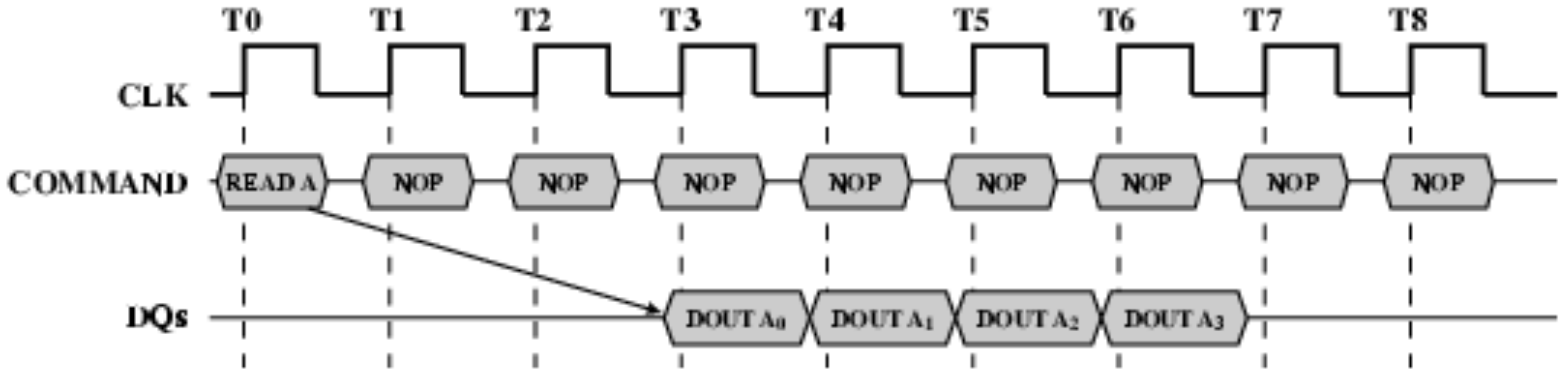
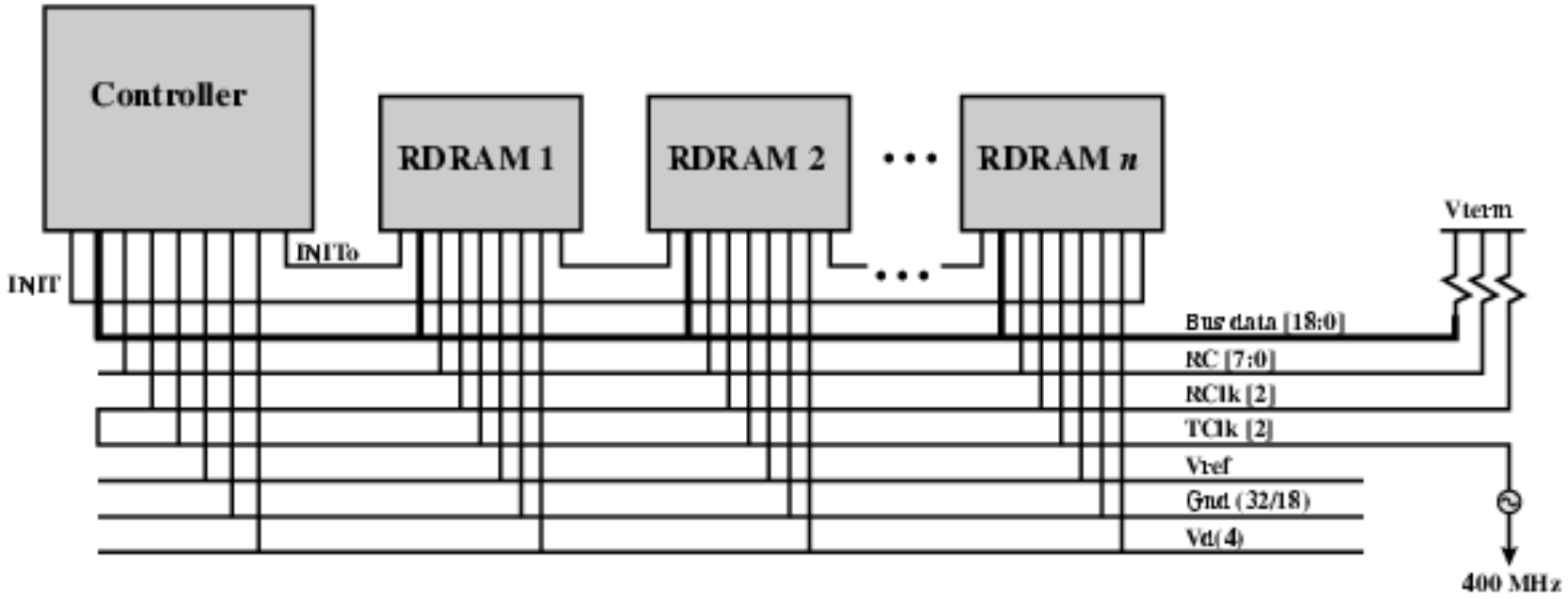


Figure 5.13 SDRAM Read Timing (Burst Length = 4, $\overline{\text{CAS}}$ latency = 2)

RAMBUS

- Adopted by Intel for Pentium & Itanium
- Main competitor to SDRAM
- Vertical package – all pins on one side
- Data exchange over 28 wires < cm long
- Bus addresses up to 320 RDRAM chips at 1.6Gbps
- Asynchronous block protocol
  - —480ns access time
  - —Then 1.6 Gbps

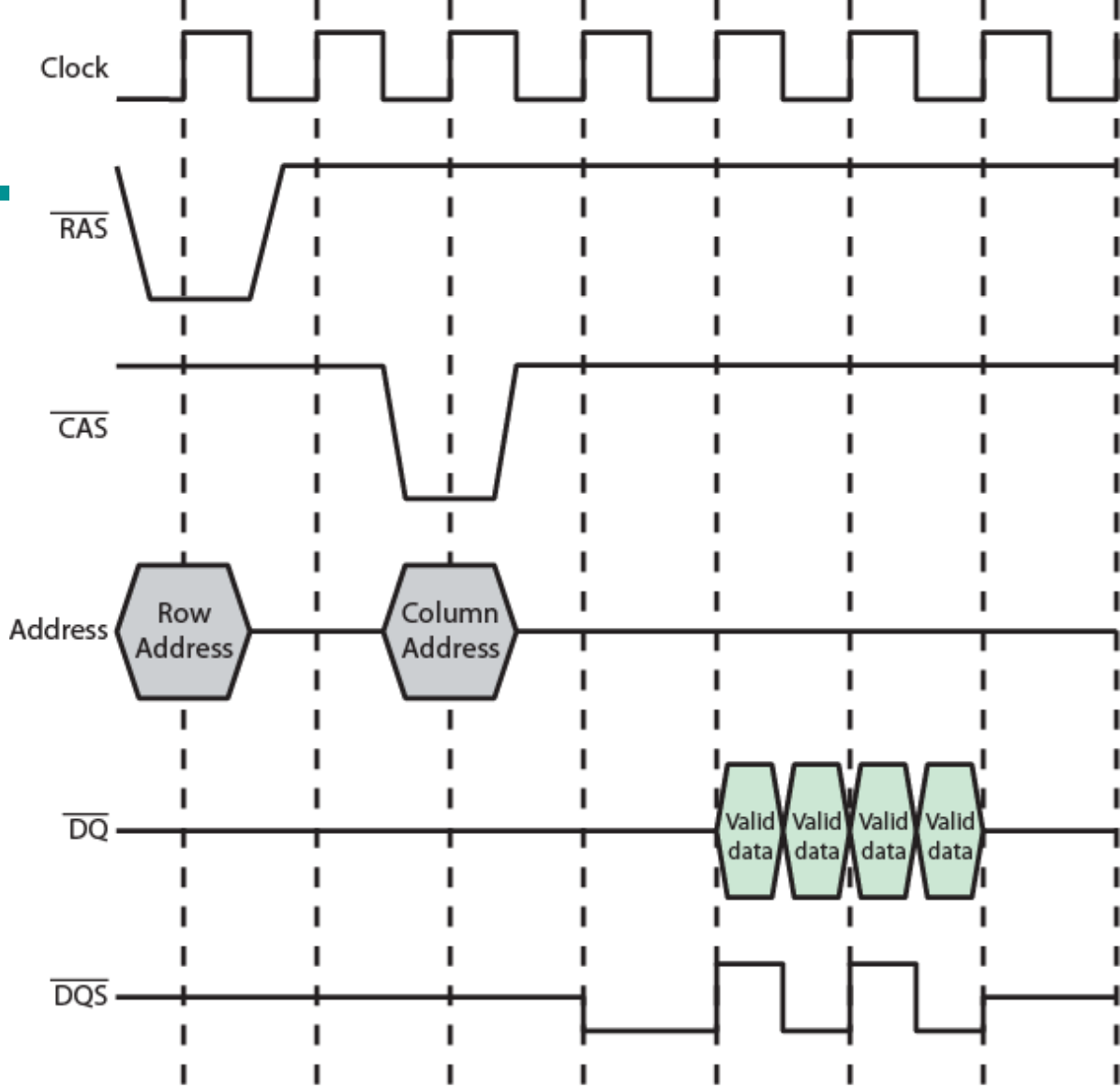
RAMBUS Diagram



DDR SDRAM

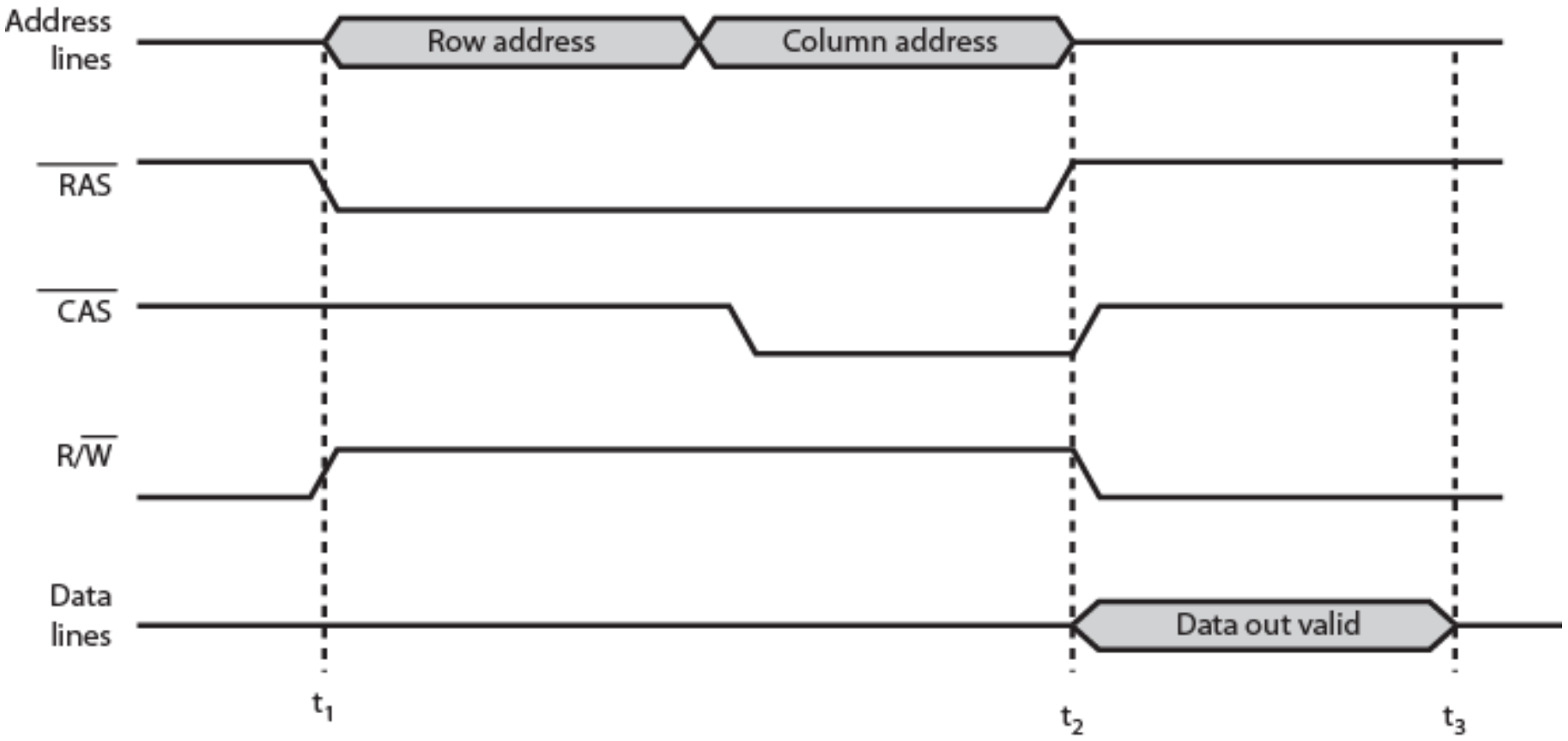
- SDRAM can only send data once per clock
- Double-data-rate SDRAM can send data twice per clock cycle
  - Rising edge and falling edge

DDR SDRAM Read Timing



RAS = row address select
CAS = column address select
DQ = data (in or out)
DQS = DQ select

Simplified DRAM Read Timing



Cache DRAM

- Mitsubishi
- Integrates small SRAM cache (16 kb) onto generic DRAM chip
- Used as true cache
  - 64-bit lines
  - Effective for ordinary random access
- To support serial access of block of data
  - E.g. refresh bit-mapped screen
    - CDRAM can prefetch data from DRAM into SRAM buffer
    - Subsequent accesses solely to SRAM

Reading

- The RAM Guide
- RDRAM